



Model 32/75 Hot Box Detector

Harmon Electronics, Inc.

Technical Reference

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Model 32 and Model 75 Hot Box Detector

Technical Reference

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This manual covers theory of operation and schematics for each of the circuit boards used in the Model 32/75 Hot Box Detector system. It also covers theory of operation for software and detailed description of the hardware/software interface. The Model 32/75 Technical Reference is designed to supplement the Model 32/75 User's Manual.

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The Universal Processor board is the control center of the HBD system. The program memories (ROMs) on this board are custom programmed to meet each customer's specific requirements. The board controls all I/O communications, controls interrupts, makes alarm decisions, performs car recognition, and handles speech.

PART ONE: PHYSICAL DESCRIPTION

The Universal Processor board has connectors P1 and SO1, switch S1, and three jumper selectable options.

Connector P1

The part of the printed circuit board which slides into the connector on the motherboard in the HBD cabinet. P1 has 72 gold-plated contact pins. All power, interrupts, data, and address lines pass through this connector.

Connector SO1

36 pin dual in line header style plug. This connector provides data, control, and communications to the time & date board.

Switch S1

SPST 4 position rocker switch that selects software dependent custom options.

Micro Monitor Jumper

The Micro Monitor jumper, if installed, disables the front panel reset function.

Off BD Jumper

The Off Board jumper must be removed or the HBD system will not operate.

EA Jumper

Jumper EA must be installed for the processor to be able to access memory external to the CPU.

PART TWO: CIRCUIT DESCRIPTION

The Universal processor board is divided into the following sections:

1. CPU Central Processing Unit
2. Address bus
3. Data bus and direction control
4. Memory
5. Reset circuit
6. Watchdog timer
7. Interrupts

Central Processing Unit (CPU)

The CPU (A1) is an Intel 8031AH processor running at 9 MHz. The processor has 128 bytes of internal memory, two 16 bit timers, four 8 bit ports, five interrupts, an 8 bit data bus, and a full duplex serial channel.

The I/O ports are the data bus, the address bus, I/O decode lines, and HBD internal bus control. These will be discussed in detail below.

The five interrupts have two levels of priority - INT0 and INT1. These interrupt priority levels are configured by software.

The processor has control lines to control the use of external memory as follows: ALE, /WR, /RD, and /PSEN. These are explained in detail in the signal description section.

For detailed information on the CPU see the Intel Embedded Microcontroller Handbook.

Address Bus

The address bus, under the control of the CPU, selects the CPU board memory, external memory, and directs data to and from the other boards in the system.

Address lines A0-A7 are latched lines from DB0-DB7. The latching is controlled by the processor with the Address Latch Enable (ALE) line.

Address lines A8-A15 originate from the CPU's I/O port P2 as P2.0-P2.7. U26 buffers this signal to the HBD internal bus.

Address lines A16-A19 originate from the CPU's I/O port P1 as P1.5-P1.8. U31 buffers this signal to HBD internal bus.

Data Bus

The data bus routes data to and from the CPU, ROM, RAM, and offboard memory, and carries unit status information, such as what triggered an interrupt.

Control Lines

The control lines aid in determining where data is routed, much in the same way an address line does. CPU I/O ports P1.0-P1.2 control U30, a 3 to 8 multiplexer that also controls U9 along with A11, A12, and A15. A15 is a 3 to 8 multiplexer that controls data bus and memory chip selection both on and off board. See signal descriptions for further information.

Memory

The board has four ROM chips (U3-U6) which contain the firmware for the HBD. The firmware consists of the core routines plus railroad specific options. The ROMs are 128K bytes in size. The RAM chips (U1-U2) are 2K X 8 static RAM chips. The RAM chips are used as a scratch pad for software and as a buffer for heat readings and axle speed.

Reset

The CPU can be reset in several ways: from the front panel switch, watchdog timer, power up, or power down.

When the Reset line is high for at least .45 milliseconds, the CPU is reset. Actuating the front panel reset switch forces this line high for 12 milliseconds. This time interval is generated by U22 (OR gate), U27 (comparator), U21 (one shot), and U27 (comparator).

The Reset line also goes high for approximately 180 milliseconds upon power down. This disables the CPU to avoid erratic operation during the low voltage condition present due to system power being turned off. The power-down circuitry monitors the HBD internal bus pin 30 (normally 12 volts). The circuitry supplies a 2.5 volt reference to U28C (comparator) and is held up by C24, a .1 μ F capacitor. The voltage is scaled down by R46 and R45 to 4 volts for the positive input to U28C. This line has a .002 μ F capacitor to allow this voltage to drop quickly. The output of U28 is normally high but goes low when the 12 volt power supply drops below 7.5 volts. The second stage of U28B, with R30 and C26 on the negative input and 2 volts on the positive input, adds a 20 millisecond hold time to the signal at this point. U28B inverts this signal making it a normally low signal.

The Reset line also goes high for 30 milliseconds upon system power up. This delays the CPU start-up until all voltages are stable. This delay is processed from U28 (comparator) with R30 and C26 setting time delay, through U22 (OR gate) for output. The output of U28A is held low for 36 milliseconds, which is 16 milliseconds longer than the reset hold off. This line is routed through U11 to the data bus. This allows the power up to be read along with S1 status.

WatchDog Timer

The watchdog timer is strobed by the CPU periodically. If the CPU does not strobe the watchdog timer for a period of 2.2 seconds, the CPU is reset.

The heart of the watchdog timer is U21, a 4060 oscillator and 14 bit ripple counter. The frequency of oscillation is 4.625 kHz. The signal goes through a 12 stage ripple counter internal to the chip, and when the 12 counter is tripped the CPU is reset. The CPU resets this chip via the MOM TMR RT line. Each time this line is strobed the 4060 is reset. While being reset the internal oscillator is disabled. This causes a slight shift in time as to the exact timing of the 2.26 second window of the watchdog. This slight time variation is always toward a longer duration and will not affect the overall operation.

Interrupts

The interrupts let the processor know when a important event has occurred, such as a wheel gate or an advance transducer signal. This will let the processor know that it needs to determine what caused this as soon as possible. Other boards can generate an interrupt to this board. The interrupt positions of these boards are jumper selectable on each board.

The interrupts come in on the HBD internal bus and go into U20 (AND gate) to choose INT 0 or 1. The interrupts are then read through U19 on the data line to determine exactly what caused the interrupt. DB0-DB3 drive /BD INT1 through U20B, and U29D DB4-DB7 drive /BD INTO through U20A and U29E.

PART THREE: SIGNAL DESCRIPTIONS

/BDPSEN	Enables the data output from the ROMs. Originates from pin 29 of A1 and is buffered by U24.
/RAMSSEL0	Selects RAM chip U1. Generated by U9 and U30 (3 to 8 address decoders).
/RAMSEL1	Selects RAM chip U2. Generated by U9 and U30 (3 to 8 address decoders).
/BDDIR	Used to read & write control RAM chips U1 & U2. Also used to latch the address lines A0-A7 from the DB0-DB7 lines. Generated by U18, U23, and U15.
/SEL-2	Used to read the status of S1, and board error conditions. Generated by U9 and U30 which are 3 to 8 address decoders.
/ISBX-SEL0	Control line through SO1 to time date board. /ISBX-SEL0 is generated by U9 and U30 which are 3 to 8 address decoders.
/ISBX-SEL1	Control line through SO1 to time date board. /ISBX-SEL1 is generated by U9 and U30 which are 3 to 8 address decoders.
MPRO	Power up indicator through SO1 to the time & date board. MPRO originates as the /DC LOW line.
/INT	Controls the cause of interrupts being read on the data bus. This is generated by U30 which is a 3 to 8 address decoder.
/OFFBOARD	
/DR	
/DIR	Used to control if data is read from or written to the HBD internal bus through J1. /DR is buffered by U25 and becomes /DIR, which is on the internal HBD bus. /OFFBOARD is generated by U33, U9, and U30. /DR is generated by U17, U18, U23, and U15.
/MEM-RQ	Generated by U30, which is a 3 to 8 address decoder, and buffered by U25.

/IO RQ

Used to control I/O operations over the internal HBD bus.

/MEM-EX

Used to control memory operations over the internal HBD bus.

/RD

Read line for the internal HBD bus. Originates on the CPU board and is buffered through U25.

/WR

Write line for the internal HBD bus. Originates on the CPU board and is buffered through U25.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

SO1 (Expansion Board Connector)

NAME	CONNECTION	DIRECTION
DB0	33	I/O
DB1	31	I/O
DB2	29	I/O
DB3	27	I/O
DB4	25	I/O
DB5	23	I/O
DB6	21	I/O
DB7	19	I/O
TXD	34	O
RXD	32	I
/RT	5	O
BDALE	6	O
/BDINT1	12	I
/BDWR	13	O
/BDINT0	14	I
/BDRD	15	O
ISBX-SEL1	20	O
ISBX-SEL0	22	O
/BDDIR	26	O
MPRO	8	O
A8	11	O
A9	9	O
A10	7	O
+5V	4,18,36	PWR OUT
+12V	1	PWR OUT
-12V	2	PWR OUT
GND	3,17,35	GND

The Digital I/O Board has the capacity to interface 24 bits of parallel Input/Output. Each input has its own protection circuit capable of passing up to 30 volts DC. The outputs are capable of sinking 200 mA with a maximum drop of 1.5 volts. In addition, two ports are capable of sourcing current through an RC network. This board also contains two Opto-Couplers that can be used to isolate any input or output circuit and an optional DPST or SPDT relay, also for isolating purposes.

PART ONE: PHYSICAL DESCRIPTION

The Digital I/O Board consists of a connector P1, connector P2, a board selection jumper and an interrupt selection jumper.

Connector P1

72 pin edge connector that slides into the motherboard in the HBD cabinet. P1 supplies all power, interrupts, data and address lines to and from the Hot Box system.

Connector P2

86 pin edge connector on the front of the board. It connects to an external connector labeled 'DIGITAL' that is routed to the terminal blocks on the HBD back panel. The P2 connector supplies all Digital input, Digital output, Opto-Coupler signals and Relay connections to the Hot Box back panel terminal blocks.

Board Select Jumpers

J3 and J4 are used to select a specific address for the Digital I/O Board. The board is normally configured with a jumper at position 0.

Interrupt Select Jumpers

J5, J6 and J7 are used to select a specific pair of interrupts for the Digital I/O Board. The board is normally configured with a jumper at across J5 and J6 at position 3 and a jumper at across J6 and J7 at position 4.

PART TWO: CIRCUIT DESCRIPTION

The Digital Board is divided into the following sections:

1. Address decoding and control signal circuit
2. Input/Output select circuit
3. Digital input buffers
4. Digital output buffers
5. Input/Output protection circuit #1
6. Input/Output protection circuit #2
7. Reset circuit
8. Opto-Isolator circuit
9. Relay circuit

Address Decoding and Control Signal Circuit

Uses a 54LS138 for U25 which decodes address lines A5, A6, and A7 to select 1 of 8 outputs. U25 is enabled by the /IO-RQ line and address line A7 from the HBD bus. The output of U25 is passed through the board select jumpers J3 and J4 to generate the signal /BD-IO-SEL. This signal is used in conjunction with the /WR and /RD signals from the HBD bus through two OR gates of U34 to generate the signals /BD-IO-WR and /BD-IO-RD. /BD-IO-SEL is also used in conjunction with the /DIR signal from the HBD bus through an OR gate of U34 to enable U27 which buffers the data lines from the HBD bus to all on board output ports. /BD-IO-RD is used to enable U28 which buffers all on board input buffer data lines to the HBD bus.

Input/Output Select Circuit

Consists of two 54LS138s for U26 and U33 along with several NOR gates from U31 and U32. U26 is enabled by the signal /BD-IO-RD and decodes address line A0, A1 and A2 to generate the select lines /IN-SEL-0, /IN-SEL-1 and /IN-SEL-2. U33 is enabled by the signal /BD-IO-SEL and decodes address lines A0, A1 and A2. The outputs of U33 are combined with the signal /BD-IO-WR through the NOR gates of U31 and U32 to generate the output select signals /OUT-SEL-0 to /OUT-SEL-6. (The output /Q3 of U33 is decoded but is not used.)

Digital Input Buffers

Consists of three 54C244 octal buffer ICs as U22, U23 and U24. Each of these ICs are selected individually for buffering data from the input circuits to the on board data lines by the signals IN-SEL-0, IN-SEL-1 and IN-SEL-2. While buffers U23 and U24 pass the data lines straight through, the signals from the input circuits must pass through a set of gates and latches before reaching buffer U22. The inputs are connected to a set of XOR gates U13 and U14, that uses its 'A' input to pass data through and its 'B' input as a control line. The signal OUT-SEL-4 latches data to U15s outputs that individually select each of these XOR gates to determine if data should pass through normally or be inverted first. The outputs of the XOR gates are connected to the 'SET' inputs of U16s and U17s R/S latches to latch an input pulse.

The signal OUT-SEL-5 latches data to U18s outputs that are connected to U16s and U17s 'RESET' inputs to individually reset a latched input pulse. The outputs of U16 and U17 are connected to buffer U22 and connected to the 'A' input of NAND gates of U19 and U20.

The signal OUT-SEL-6 latches data to the outputs of U21 which are connected to the 'B' inputs of U19 and U20 to individually select any of the inputs to cause an interrupt. The outputs of U19s NAND gates are tied together to generate the /BD-INT-1 which is routed through jumper J7 to the off board interrupt signals /INT-0 to /INT-7. The outputs of U20s NAND gates are tied together to generate the /BD-INT-2 which is routed through jumper J5 to the off board interrupt signals /INT-0 to /INT-7.

Digital Output Buffers

Consists of three 74C373 octal buffer/latch ICs as U6, U9 and U10. Each of these ICs are selected individually for latching data from the on board data lines to the output circuits by the signals OUT-SEL-0, OUT-SEL-1 and OUT-SEL-2. The outputs of these ICs are enabled by the RT signal which only goes high during a reset allowing all outputs to cleared.

Input/Output Protection Circuit #1

Consists of transistor QA, comparator UA, resistors RA to RG, capacitor CA, and diodes CRA and CRB. The output lines of U6, U9 and U10 enter the circuit through resistor RG to the Base of transistor QA with resistor RF tied to ground. This signal is inverted through QA and is finally output through resistor RA to the terminal block connector.

When a signal is input from the terminal block connector it first passes through resistor RA and RC to the minus input of comparator UA. CRB is a Zener diode used for excessive voltage protection while diode CRA and resistor RB will route negative voltages to the +12 volts. Resistor RC helps to limit current going to the comparator while resistor RD and capacitor CA for an R/C time constant to help absorb any high frequency spikes and transients. The Plus input of the comparator is connected to a voltage divider set up with resistors R50 and R51 to establish a reference voltage of 0.5 volts.

The comparator is setup in an inverting configuration so that when the input voltage is below the reference voltage of 0.5 volts the output will be pulled to +5 volts through resistor RE. When the input voltage exceeds the reference voltage of 0.5 volts the output goes to ground. This output is then connected to the input buffers ICs.

Input/Output Protection Circuit #2

Used on two of the 24 input/output circuits and will be described with the components of P2.7 of the terminal block connector. This circuit consists of transistors Q24, Q27 and Q28, a comparator of U12, several resistors, capacitor C23, and diodes CR30 and CR56. The output lines of U24 enter the circuit through R83 to the Base of Q27 with R77 tied to ground. This signal is inverted through Q27 and is used to sink up to 200 mA of current through R33 to the terminal block connector. To source current, the output of buffer U24 enters the circuit through R85 to the Base of Q24 with R68 tied to ground. The signal is inverted through Q24 and passes through R70 to the Base Q25 which inverts the signal again and outputs through R33 to the terminal block. R78 and R71 are tied to the terminal block to allow the user to specify an input voltage.

When a signal is input from the terminal block connector it first passes through R33 and R48 to the '-' input of comparator UA. CR30 is a Zener diode used for excessive voltage protection while CR56 and R47 will route negative voltages to the +12 volts. Resistor R48 helps to limit current going to the comparator while R49 and C23 for an R/C time constant to help absorb any high frequency spikes and transients.

The '+' input of the comparator is connected to a voltage divider set up with resistors R50 and R51 to establish a reference voltage of 0.5 volts. The comparator is setup in an inverting configuration so that when the input voltage is below the reference voltage of 0.5 volts the output will be pulled to +5 volts through resistor R55. When the input voltage exceeds the reference voltage of 0.5 volts the output goes to ground. This output is then connected to the input buffers ICs.

Reset Circuit

Consists of a NOR gate of U31, three resistors and a capacitor. The signal /RESET from the HBD bus is inverted through the NOR gate of U31 and passes through the resistors R60 and R58 with R59 pulled to +5 volts and C31 tied to ground. This forms an RC time constant to keep the signal stable at a logic high during a system reset. The duration is long enough to allow the processor to set the outputs to known condition after the system has been reset or powered up.

Opto-Isolator Circuit

Consists of U1 and U3 opto-coupler ICs along with several resistors and diodes. Resistors R10, R11, R24 and R25 are used for current limiting with diodes CR2 and CR6 for reverse voltage protection on the LED emitters of the opto-coupler ICs. On the transistor side of the opto-couplers, resistors R9 and R23 are used for current limiting and Zener diodes CR1 and CR5 are used for over-voltage protection.

Relay Circuit

Reed style relay with each of its pin routed directly to the card edge connector P2. The relay has no electrical connections with the Digital I/O Board and is intended for isolating control signals into or out of the board. The Digital I/O board has a socket for selecting either a DPST or SPDT type relay.

PART THREE: SIGNAL DESCRIPTIONS

/WR	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /WR is used to control Write operations to the on board output ports.
/RD	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /RD is used to control Read operations from the on board input ports.
/DIR	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /DIR is used in conjunction with /RD and /WR for input/output port operations.
/BD-IO-WR	This signal is generated on this board and is used for writing data to the digital output buffers and other on board control circuits.
/BD-IO-RD	This signal is generated on this board and is used for reading data from the digital input buffers.
/BD-IO-SEL	This signal is generated on this board and is used to enable U26 and U33 address decoders and to generate the signals /BD-IO-WR and /BD-IO-RD.
/IN-SEL-0 to 2	This signal is generated on this board and is used to select an one of the input data buffer ICs U22, U23 or U24.

- /OUT-SEL-0 to 2** This signal is generated on this board and is used to select one of the output data buffer ICs U6, U9 or U10.
- /OUT-SEL-4 to 6** This signal is generated on this board and is used to select one of the latching buffer ICs U15, U18 or U21 that inverts input data, latches input data or enables input data to cause an interrupt.
- /BD-INT-1** This signal is generated on this board and is used to select one of eight interrupts labeled /INT-0 to /INT-7 which is selected by placing a jumper across J6 and J7.
- /BD-INT-2** This signal is generated on this board and is used to select one of eight interrupts labeled /INT-0 to /INT-7 which is selected by placing a jumper across J5 and J6.
- RT** This signal is generated on this board and is used to keep the output circuits stable at a logic high during a system reset. This gives the processor time to set the outputs to known condition after the system has been reset or powered up.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

Digital I/O Board P2 Connector

NAME	CONNECTION	TERMINAL BLOCK
P0.0	1	TB10-1
P0.1	2	TB10-2
P0.2	3	TB10-3
P0.3	4	TB10-4
P0.4	5	TB10-5
P0.5	6	TB10-6
P0.6	7	TB10-7
P0.7	8	TB10-8
P1.0	13	TB12-1
P1.1	14	TB12-2
P1.2	15	TB12-3
P1.3	16	TB12-4
P1.4	17	TB12-5
P1.5	18	TB12-6
P1.6	19	TB12-7
P1.7	20	TB12-8
P2.0	32	TB14-8
P2.1	33	TB14-9
P2.2	34	TB14-10
P2.3	35	TB14-11
P2.4	36	TB14-12
P2.5	37	TB15-1
P2.6	38	TB15-2
P2.7	39	TB15-3
Opto Collector	9	TB10-9
Opto Emitter	10	TB10-10
Opto + Input	12	TB10-12
Opto - Input	11	TB10-11
Opto Collector	28	TB14-4
Opto Emitter	29	TB14-5
Opto + Input	31	TB14-7
Opto - Input	30	TB14-6
Relay NO1	22	TB12-10
Relay Contact 1	24	TB12-12
Relay NO2	23	TB12-11
Relay Contact 2	25	TB14-1
Relay Coil	26	TB14-2
Relay Coil	27	TB14-3
R73	40	TB15-4
R71	41	TB15-5
Power	42	TB15-6
GND	43	TB15-7

The Display Board is the primary method by which a Hot Box System is controlled and information about the system is retrieved. The LED character displays are used to display system parameters and system setup configurations. The Rotary switch, toggle switches and dip switches are used to select modes of operation, reset the system, and provide on-site system configuration.

PART ONE: PHYSICAL DESCRIPTION

The Display Board consists of connector P1, a board selection jumper, a 16 position rotary switch, a 3 position toggle switch, two self centering toggle switches, two 8 position DIP switches, two 4 character 16 segment LED displays, and 8 LED indicator lights. Attached to the Display Board is a HBD bus card extender that provides easier access to the bus for testing purposes.

Connector P1

The part of the printed circuit board which slides into the connector on the card extender that is plugged into the motherboard in the HBD cabinet. P1 has 72 gold-plated contact pins. All power, interrupts, data, and address lines pass through this connector.

Board Select Jumper

Used to select a specific address for the Display Board. The board is normally configured with a jumper at position 5.

16 Position Rotary Switch

Used to turn the display off or to select from either 5 standard modes of operation or 6 customer specified modes.

3 Position Toggle Switch

Used to select individual features of each mode of operation.

Self Centering Toggle Switches

Used to select individual features of each mode of operation.

8 Position DIP Switches

Used to select from a group of customer specified setup parameters.

4 Character 16 Segment Displays

Used to retrieve information from the Hot Box system and show system setup parameters.

8 LED Indicators

Used to display system port information or wheel gate and alarm information during train passage.

PART TWO: CIRCUIT DESCRIPTION

The Display Board is divided into the following sections:

1. Address decoding circuit
2. Input/Output select circuit
3. Display output buffers
4. Switch input buffers

Address Decoding Circuit

Uses a 54LS138 which decodes address lines A5, A6, and A7 to select 1 of 8 outputs. U1 is enabled by the /IO-RQ line from the HBD bus. The output of U1 is passed through the Board Select jumper to generate the signal /BD-SEL.

Input/Output Select Circuit

Consists of U2 which is a 3 line to 8 line demultiplexer, U3 (OR gates), U12 (OR gates) and a NOR gate from U4. U2 is enabled by signal /BD-SEL and decodes address lines A2, A3 and A4. The decoded outputs Q0-Q3 of U2 are combined with the signal /BD-WR through U3 to generate the select signals for the 4 character 16 segment displays. The Q4 decoded output of U2 is combined with the signal /BD-WR through U4 to generate the signal /SEL-4-WR. The Q0-Q2 decoded outputs of U2 are combined with the signal /BD-RD through U12 to generate the signals /SEL-0-RD, /SEL-1-RD and /SEL-2-RD. The signal /BD-WR is generated by combining the signals /WR and /BD-SEL through an OR gate of U8.

Display Output Buffers

Consist of U5 and U6. U5 buffers data from the HBD system bus to the four character 16 segment displays and the LED Indicator lights. U5 is enabled by a signal that is generated from combining the signals /BD-SEL and /DIR through an OR gate of U12. The four character 16 segment displays are selected by address lines A0 and A1 which are buffered from the HBD system bus through two OR gates of U8. The displays are write enabled from the select lines of U2 through OR gates of U3. The Display Board is capable of using 4 of the four character 16 segment displays, but only 2 four character displays are installed in the current Hot Box system. U6 latches data output from U5 to the 8 LED Indicator lights and is enabled by the signal /SEL-4-WR. Resistor pack R7 is used for limiting the current to the 8 Indicator lights. Resistor pack R6 is used to pull up the output lines of U5.

Switch Input Buffers

Consist of U7, U9, U10 and U11. The signal /SEL-0-RD is used to enable reading of the inputs of U9 data buffer. U9 inputs the switch settings of the 16 position rotary switch along with the 3 position switch and the two self centering switches. The signal /SEL-1-RD is used to enable reading of the inputs from U11 data buffer. U11 inputs the switch settings of DIP switch number 1. The signal /SEL-2-RD is used to enable reading of the inputs from U10 data buffer. U10 inputs the switch settings of DIP switch number 2. The outputs of U9, U10 and U11 are passed through U7 data buffer. U7 is enabled by the signal /BD-RD which is generated by combining the signals /RD and /BD-SEL through an OR gate of U8. Resistor packs R8, R10 and R11 are used to pull up the input lines of U9, U10 and U11.

PART THREE: SIGNAL DESCRIPTIONS

- /WR** This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /WR is used to control Write operations to the on board output ports.
- /RD** This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /RD is used to control Read operations from the on board input ports.
- /DIR** This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /DIR is used in conjunction with /RD and /WR for on board input/output port operations.
- /BD-WR** This signal is generated on this board and is used for writing data to the 4 character 16 segment displays and the 8 Indicator lights.
- /BD-RD** This signal is generated on this board and is used for reading data from the input switches of the front panel.
- /BD-SEL** This signal is generated on this board and is used to enable the address decoder (U2) and to generate the signals /BD-WR and /BD-RD.
- /SEL-4-WR** This signal is generated on this board and is used to enable the data buffer (U6) for latching data to the LED Indicator lights.
- /SEL-0-RD** This signal is generated on this board and is used to enable the data buffer (U9) for latching data from the rotary and toggle switches of the front panel.
- /SEL-1-RD** This signal is generated on this board and is used to enable the data buffer (U11) for latching data from DIP switch number 1 of the front panel.
- /SEL-2-RD** This signal is generated on this board and is used to enable the data buffer (U10) for latching data from DIP switch number 2 of the front panel.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

The Speech ROM / Memory Board consists of a bank of 16 sockets for the Speech data ROMs, a bank of 16 sockets for RAM memory chips used to store user recordable Speech and a battery backup circuit to save the contents of the RAM memory during power downs and power outages. The RAM chips are not normally present as the user speech recording feature is not implemented in the current production boards.

PART ONE: PHYSICAL DESCRIPTION

The Speech ROM / Memory Board contains a connector P1, five jumper selections, two memory protection jumpers, a memory installation jumper and a battery test point.

Connector P1

The part of the printed circuit board which slides into a connector on the motherboard in the HBD cabinet. The P1 connector has 72 gold plated contacts which supply all power, interrupts, data and address lines to the Hot Box system.

Jumper J1

Used in the RAM memory address decoding to select a different address range for a multi-board configuration. It is normally configured with a jumper across A-B and a jumper across C-D.

Jumper J2

Used in the RAM memory address decoding to select a different address range for a multi-board configuration. It is normally configured with jumpers at position C and position D.

Jumper J3

Used in the Speech ROM address decoding to select a different address range for a multi-board configuration. It is normally configured with a jumper at position A.

Jumper J4

Used in the RAM memory selection logic for selecting as normal or expanded memory. Normally jumpered at position A-B.

Jumper J5

Used in the Speech ROM selection logic for selecting as normal or expanded memory. Normally jumpered at position A-B.

Memory Protection

Jumper used to Write Protect the RAM memory banks.

Memory Installation

Jumper used to clear the RAM memory banks by placing a jumper across this connection for approximately 10 seconds.

Battery Test Point

Used to test the battery that backs up the RAM memory banks.

PART TWO: CIRCUIT DESCRIPTION

The Speech ROM / Memory Board is divided into the following sections:

1. Speech ROM memory Address decoding
2. Speech ROM memory banks
3. Memory buffer circuits
4. Battery backup circuit

Speech ROM Memory Address Decoding

Utilizes address decoders U3 and U6, which decode address lines A14, A15, A16 and A17. U3 and U6 are enabled through jumper J3 signal /BD-ROM-ADR from U9 address decoder that decodes address lines A18 and A19. U9 is enabled through jumper J5 from signals /MEM-RQ or /MEM-EX. U3, U6 and U9 are 54LS138 de-multiplexers which decode 3 lines to 8 lines and are enabled by one active high line and two active low lines. U4 is a 54LS32 quad OR gate of which one gate inputs the signal /RD to generate signal /BUF-RD. Two more OR gates of U4 input the signals /BUF-RD and /BD-ROM-ADR to generate signals /BD-ROM-RD1 and /BD-ROM-RD2. The signal /BD-ROM-RD1 is used to enable U2 data line buffer and /BD-ROM-RD2 is used to enable the Speech ROM banks.

Speech ROM Memory Banks

2764 (8K) or 27128 (16K) EPROMs that contain digitally recorded speech patterns. Each EPROM is capable of storing from 1 to 9 words or phrases that can be selected for speaking by the Hot Box Detector. These ROMs are labeled as ROM0 - ROM15.

Memory Buffer Circuit

Consists of U1, U2 and U5, which are 54LS244 octal buffers. U1 and U5 buffer Address line A0 - A15 and use resistor packs R16 and R21 to pull up the output lines. U2 buffers the Data lines to the Speech Rom chips and uses resistor pack R18 to pull up the output lines. U15 is a 54LS245 bi-directional octal buffer that buffers the data lines to the RAM memory banks and uses resistor pack R26 to pull up the data lines between the buffer and RAM memory banks.

Battery Backup Circuit

Consists of transistors Q1 and Q2, temperature sensor RT1 and zener diodes CR1 and CR2 along with R6, R14 and R15 as bias resistors. The temperature sensor RT1 is used for temperature compensation for maintaining optimum trickle charge current under varying temperature conditions. The battery used in this circuit is a nickel-cadmium 3.6 volt cell used to maintain the speech stored in the RAM memory banks. The battery is also usually left off of the board since the RAM recording feature is not enabled at this time.

PART THREE: SIGNAL DESCRIPTIONS

/MEM-RQ	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /MEM-RD is used to synchronize Normal memory operations.
/MEM-EX	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /MEM-EX is used to synchronize Extended memory operations.
/WR	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /WR is used to control Write operations to the RAM memory banks or to output ports.
/RD	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /RD is used to control Read operations from the RAM memory banks or from input ports.
/DIR	This signal is generated on the Universal Processor Board and is interfaced to this board via P1. /DIR is used in conjunction with /RD and /WR for memory and input/output port operations.
MPRO	Power up indicator from the Universal Processor board. MPRO is held low for 62 milliseconds upon power up to allow the circuits to stabilize. When low, it turns off Q3, preventing the +5 volt power supply from reaching U7. This prevents accidental writes to the RAM memory banks.
/BD-RAM-DIR	This signal is generated on board and is used to control direction of the Data lines through buffer U15 that buffers data to and from the RAM memory banks.
/BD-RAM-ADR	This signal is generated on board and is used to enable the data buffer U15 and is used in the Write Protect circuit for the RAM memory banks.
/BD-RAM-SEL1	This signal is generated on board and is used to enable the memory chips RAM0 - RAM7.
/BD-RAM-SEL2	This signal is generated on board and is used to enable the memory chips RAM8 - RAM15.

/BD-RAM-SEL-GRP1

This signal is generated on board and is used to enable the address decoder U12 which generates the select signals for memory chips RAM0 - RAM7.

/BD-RAM-SEL-GRP2

This signal is generated on board and is used to enable the address decoder U13 which generates the select signals for memory chips RAM8 - RAM15.

/BUF-RD

This signal is generated on board and is used in the enable and direction control signals for U15 data buffer.

/RAM-SEL-0 TO 15

These signals are generated on board by U12 and U13 and are used to select the individual memory chips RAM0 - RAM15 of the RAM memory banks.

MEM+

Battery back up power. When system power is present, this voltage is supplied by Q1 & Q2 which derive the power from +5 volts. This voltage also keeps the nicad battery charged. RT1 regulates the current to the battery with changes in temperature to give the correct charge rate.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

Speech Board

HPN 225815-000

The speech board provides a means for the HBD to communicate directly with the train crew. The board produces computer generated speech from a predefined vocabulary. The board can activate a radio and broadcast over the radio to the train crew. The speech board also has external I/O lines, a relay, and an optical coupler.

PART ONE: PHYSICAL DESCRIPTION

The speech board has connectors P1 and P2, switches S1-S3, jumper selectors J1 and J2, pots R123 and R122, and speaker jack J3.

Connector P1

The part of the printed circuit board which attaches to a cable labeled 'SPEECH'. This cable is connected to the terminal blocks on the rear of the HBD cabinet. P1 has 72 gold-plated pins. The voice output, external I/O radio RCVR input, optocoupler connections, and relay connections are all routed through this connector.

Connector P2

The part of the printed circuit board which slides into the connector on the motherboard in the HBD cabinet. P2 has 72 gold-plated pins. All power, interrupts, data, and address lines pass through this connector.

Switch S1

8 position dip switch used to set the mile post voice location. S1 controls the tenths and units numbers.

Switch S2

8 position dip switch used to set the mile post voice location. S2 controls the tens and hundreds numbers.

Switch S3

4 position dip switch used to select railroad specific options as determined by the software.

Jumper J1

Used to select the board address (see details below on U22 and BD IO Sel).

Jumper J2

Used to set interrupt priority level of interrupts generated by the speech board.

Pot R123

Used to adjust the clock frequency. This sets the clock used to generate speech. This is factory set and should not be adjusted in the field.

Pot R122

This is used to set the volume of the speech produced on the HBD built in speaker. This pot may be adjusted in the field to meet the needs of the location in which the HBD is installed. This pot does NOT affect the volume of the speech broadcast over the radio to train crews.

J3 Speaker Jack

Connects the speaker on the HBD cabinet to the speech board.

PART TWO: CIRCUIT DESCRIPTION

The speech board is divided into the following sections:

1. Speech decoder
2. Speech decoder bus interface logic
3. Analog speech amplifier
4. Speech low pass filter
5. Speech clock
6. Level sensing
7. Pause detect
8. Squelch detect
9. Input data buffers
10. Output data buffers
11. Bus interface logic
12. Interrupts
13. Shift registers
14. Address decode
15. External I/O
16. Relay
17. Optical coupler

Speech Decoder

The speech decoder U38 (MC3517L) takes a serial sting of digital data and converts it to speech. The digital serial string input is on pin 13. This is clocked in by the speech clock on pin 14.

Pin 15 determines whether the unit decodes or encodes speech. When pin 15 is low, U38 will decode the digital speech input. When high, the speech board does not encode speech because the input circuitry has been removed. The current software does not support this function.

R95, R96, and C58 set the frequency of the syllabic filter. This filter helps to control the rise and fall times of the spoken word. Pin 11 is part of this circuit which puts a varying width pulse out into the filter input on pin 3. Whenever the U26 detects a pause in the speech pin 11 is pulled high through CR25.

R106, R107, and C61 are connected between the pin 7 analog output and the pin 6 filter input to provide a integrating filter for the voice.

Gain control is provided by U28, CR18, CR19, R87, R88, R91, R90, R93, R94, and C55. This is input to pin 4 of U38.

Speech Decoder Bus Interface Logic

U32, an MC14014B parallel to serial converter, takes the digital word and converts it to serial to drive the speech decoder described above via the PB serial speech data line. When U32's P/S pin is high, it is taking in parallel data; when it is low, it is shifting the parallel data to serial data with the rising clock pulse. The RCD serial speech data line into U32 was the field recorded speech from the speech encoder. This function is not available and this line is not used at current time.

U32 receives the parallel 8 bits of speech data from a 54HC373 8 bit latch (U31). The latch is enabled by OUTSEL0.

The U32 latch is enabled by OUTSEL0 when low data at the output is latched. This line is generated by U24 (OR gate), U28, and U22 (3 to 8 multiplexer).

Analog Speech Amplifier

The analog speech amplifier (U37) is an LM380 audio power amplifier, used to drive the HBD speaker for internal use. This amplifier does not affect the speech broadcast to the train crew. It has an internal gain setting of 34 dB and is capable of driving low impedance loads.

The volume pot (R122) serves as a voltage divider of the signal before it is amplified by U37. This only affects the attenuation of the circuit and not the gain of the circuit.

Q9 (a 2N4400) is used to shunt out the signal to U37 giving a pulsed affect. Q9 is normally off and has no effect. This is true only in the voice applications. In certain railroad specific software, a test tone is available. In this application, this transistor is pulsed on for short periods of time. The control line to Q9 is test speaker from U34 bit 5.

C71 (.0022 μ F) and R117 (1k) form a low pass filter on the input of U37 (LM380). This is to help filter out high frequency noise and improve the quality of the voice.

The output of U37 is biased at approximately 6 volts DC. C75, a 140 μ F capacitor, is used to AC couple the speech to the speaker.

The speaker is not on the speech board - it is located in the front cover of the Hot Box Detector.

Speech Low Pass Filter

The speech low pass filter is an active filter that rolls off at 3 kHz and has a gain of +.5db. The speech leaves the decoder (U38) and is ac coupled through C60 (1 μ F capacitor) into the low pass filter.

U28 C & D make up the low pass filter. R80 - R86, R98 and C63 - C66 set the cutoff frequency of the low pass filter.

Speech Clock

The speech clock is developed by U29 (4047 oscillator). The frequency is set by R108, R123, and C67. The frequency is adjusted by R123 to give a speech clock output from U29 of 30 kHz $\pm$ 300 Hz. This is a factory set adjustment that should not be modified in the field.

The speech clock line also drives U38, U14, U18, U32 and U15. U14 and U15 are no longer used as they were part of the speech encoder circuit that is no longer in use.

The speech clock line drives the speech decoder chip (U38) which establishes the reconstructed speech rate.

The speech clock line drives the parallel to serial converter chip (U32). This assures that the serial speech data is synchronous to the speech decoder chip.

The speech clock line drives U18 (14022 octal divider). U18 divides the frequency by 8. If the frequency input is 30 kHz, the output frequency (pin) 2 is 3.75 kHz. The output is a square wave with an on time of 33 microseconds and an off time of 234 microseconds.

Level Sensing

The level sensors sense the speech level and set a bit if it meets certain parameters or there is a pause in speech. The unit also monitors the radio to make sure there is no activity and sets a digital bit if the channel is clear.

U26 (LM239 comparator) sections A & B were used to monitor the speech encoder level. The output of this section is 500mv. However, since the speech encoder is not used, this circuitry does not have an output.

U25 (LM239 comparator) sections C & D are used to monitor the speech output from the low pass filter discussed above. When the board is speaking, the voltage will be greater than 500 millivolts. If this is the case, the output is considered high and is sent to the Universal Processor Board via buffer U1. The input is biased at approximately 5.6 VDC and the reference comparator (pin 8) is at 5.1 VDC. This is scaled down from the input by R44 and R45. C31 (1 μ F capacitor) is used to remove the AC, or voice component, from reference pin 8. When the voice signal reaches .5 volts peak, the output of comparator will go low.

The second stage adds a delay to the results of the first comparator. This is done through the time constant from R43 and C30. This adds approximately 20 milliseconds of delay. This delay provides a stable logic output that does not bounce with each spoken word. The reference pin of the second stage (U25, pin 11) is biased at 2.5 VDC.

Pause Detect

U26 (LM239 comparator) sections C & D check for a pause in the spoken message. When a pause is found, the output is high, driving buffer U10 bit 2. The input is the speech output from the low pass speech filter described above. The positive input (pin 9) to U26 is biased at 5.6 VDC. The reference pin is biased at 5.5 volts DC. This is set by voltage divider R49 and R51.

This will enable the detector to sense an amplitude of .1 and above in the speech. The ac voltage on the reference pin is filtered by C53 to provide a stable reference voltage. The output of the first stage is normally high (no speech) and goes low when speech is present. The output of pin 14 drives the speech decoder (U38) pin 11 via blocking diode CR25.

R46, R56, R47, and C32 offer a time delay to the second stage of the pause comparator. The speech pause output is delayed approximately 30 milliseconds. When speech starts, it is delayed 9 milliseconds. This delay stage provides a smoothing effect on the output so that it does not jump up and down at each symbol.

Squelch Detect

The squelch detect monitors the input (P1-28) from the radio audio line. When no voice is present, the output of the squelch detect to U10 bit 0 is low. This tells the universal processor board that the radio channel is free for broadcast.

The input goes through a 100 Hz to 1 kHz bandpass filter. This filter consists of R35, R37, R36, C25, C26, and C27. A DC bias is applied to the input by R38 and R36. This bias is approximately 4.6 VDC on the non inverting pin (7) of U25.

The reference pin of U25 is pin 6. It is biased by R55 and R54 which scale down the input on pin 7 by .1 VDC. In this case the voltage will be approximately 4.5 VDC. The AC signal is filtered off this pin by C25.

The output of the 1st stage is normally high (when no speech is detected on the radio) and low when it detects speech on the radio.

R53 and C34 add a delay of approximately 20 milliseconds to the output of the first stage. This helps to keep the output constant with changes in speech.

The reference pin of the second stage (U25 pin 5) is biased at 2.5 VDC.

The output of the second stage (U25 pin 2) is normally low (when no speech is detected on the radio), and high when radio speech is detected.

Input Data Buffers

The data into the speech board comes from the Universal Processor Board and enters through P2 DAT0 to DAT7. The input is buffered through U33 (74LS244 line receiver). The output from U33 is called D0 out to D7 out (the 'out' notation refers to the direction relative to the Universal Processor Board - in this case, out of the Universal Processor board).

U33 is enabled when enable pins 1 and 19 are low. When the enable pins are high, the output is placed into a high-impedance state. These pins are controlled by /DIR ORed with /BD IO SEL. When both these lines are low, the chip is selected.

Input Data Buffer to Output Port

The output port buffer is U7 (74LS373). The input to U7 comes from U33 (described above). The output from U7 is D0'OUT to D7'OUT.

U7 is controlled by the OUTSEL2 line. When high the data is allowed to flow through; when low, the current data is latched. The output of U7 is controlled by the RT line which, when low, will allow the data to flow through.

The RT line comes from U24 (NOR gate D). This functions as a inverter for the /RESET line. The /RESET line is generated on the universal processor board. The RT line will prevent U7 from writing false data at such times as power up or down or when system is resetting.

The OUTSEL2 line is generated by U24, U23, U22, and U35 which is part of the address decoding logic. See bus address decoding below for details below.

Input Data Buffer to Speech Decoder

U31 (54LS373) buffers D0OUT to D7OUT for the speech decoder. The output of U31 is directed into a parallel to serial converter (U32). See above (speech decoder bus interface logic) for a detailed explanation of U32 and related circuits.

U31 is controlled by line OUTSEL0. When high, data will flow through U31; when low, the data is latched. OUTSEL0 is generated by U24, U23, U22, and U35. See bus address decoding (below) for details.

Input Data Control Lines

U34 (54LS373 buffer) interfaces D0OUT - D7OUT to various control lines. This chip is controlled by OUTSEL1. When OUTSEL1 is high, data will flow through U34; when it is low, the data is latched. OUTSEL1 is generated by U24, U23, U22, and U35. See bus address decoding (below) for details.

Bit 0 out of U34 is BD INT EN 1 and is used to enable or disable the capability of the speech board to produce an interrupt to the system. The line controls U36 (NAND gate) if this line is high interrupts are enabled.

Bit 4 out of U34 is RCD/PB CNTRL. It controls the speech decoder (U38). When this line is low, the Speech decoder is placed in the decoder mode.

Bit 5 out of U34 is Test speaker (mute Cntrl). This line will disable speech output from HBD speaker when high. Note this has no effect on radio broadcasts to trains - it will only affect voice from the HBD speaker.

Bit 7 out of U34 is AMP TEST. This tests the squelch detect circuit discussed earlier. This is used as part of the board self test.

Output Data Buffers

The data out of the speech board goes to the Universal Processor board via P2 DAT0-DAT7. The output is buffered through U33 (74LS244 line driver). Input to U20 is called D0IN to D7IN (the notation 'IN' refers to the direction relative to the Universal Processor board). U20 is enabled by /BD IO RD which is generated by U35. For a better definition of /BD IO RD, see bus address decoding (below).

Output Data Buffer Speech Encoder

U12 is one source of input for U20 (D0 IN - D7 IN). This was used to carry encoded speech data. Since this board is no longer used to encode speech, this part is not present on most speech boards.

Output Data Buffer Level Detects and S3

U10 (54C244) buffer supplies U20 with data (D0 IN - D7 IN). This carries comparator outputs @500 millivolts, pause detect, squelch detect, and S3 status information to the Universal Processor board.

The output of U10 is controlled by /IN SEL 1 which is generated by U19 and U35. See bus address decoding (below) for information on U19 and U35.

Output Data Buffer Mile Post Tenths and Units Settings

U11 (54C244 buffer) interfaces S1 settings to U20 via D0 IN - D7 IN. U11 is controlled by /IN SEL 3. When /IN SEL 3 is low it enables the output of U11.

S1 is divided into two groups of 4 bits with positions 1 to 4 being the tenths and 5 to 8 being the units. The coding is binary with the following decoding:

Switch position	value
Tenths	
1	1
2	2
3	4
4	8
Units	
5	1
6	2
7	4
8	8

Output Data Buffer Mile Post Tens and Hundreds Settings

U16 (54C244 buffer) interfaces S2 settings to U20 via D0 IN - D7 IN. U16 is controlled by /IN SEL 4. When /IN SEL 4 is low, it enables the output of U16. /IN SEL 4 is generated by U19 and U35. For details, see bus address decoding (below).

S2 is divided into two groups of 4 bits with positions 1 to 4 being the tens and 5 to 8 being the hundreds. The coding is binary:

Switch position	value
Tens	
1	1
2	2
3	4
4	8
Hundreds	
5	1
6	2
7	4
8	8

PART THREE: BUS ADDRESS DECODING

/BD IO SEL

U22 (54LS138 3 to 8 multiplexer) and J1 determine the decoding of /BD IO SEL. J1's position determines which decoder is used. Normally, J1 is in the A position, which is the Q0 output of U22. Address line ADR7 must be low and the IORQ line must be high for U22 to be selected. These lines originate on the Universal Processor board.

Address lines ADR4, ADR5, ADR6 are the address lines to U22. These originate on the Universal Processor board. With J1 set to the A position the lines ADR4, ADR5, and ADR6 must all be low.

OUT SEL decoding

U23 (54LS138 3 to 8 multiplexer), U24, and U35 determine the states of the OUT SEL 0 - OUT SEL 2 lines. U23 outputs are controlled by the /BD IO SEL line described above. When /BD IO SEL is low, U23's outputs are enabled.

U23 uses ADR0, ADR1, and ADR2; however, only ADR0 and ADR1 have an effect on the output selected in this case.

U23 output bits 0-2 drive U24 (NOR gate), with bit 0 controlling line OUT SEL 0, bit 1 controlling OUT SEL 1, and bit 2 controlling line OUT SEL 2.

The output from U24 is controlled by the /BD IO WR line which is generated by U35 (OR gate). /BD IO SEL is logically ORed with /WR from the Universal Processor board. The line /BD IO WR must be low for U24 to have an active output.

IN SEL Decoding

U19 (54LS138 3 to 8 multiplexer) and U35 determine the states of the IN SEL 0-IN SEL 4 lines. U19 output is controlled by the /BD IO RD line which is generated by U35 (OR gate). /RD from the Universal Processor board is logically ORed with /BD IO SEL (described above). When this result is low, U19 output is enabled.

U19 uses ADR0, ADR1, and ADR2 from the Universal Processor board to select which IN SEL line is selected (active low).

Interrupts

The interrupts provide a timing pulse back to the Universal Processor board when the 8 bits of speech data have been serially shifted.

U18 supplies the pulse to the U21 (14013B D flip flop) clock input. When the clock goes high the output goes high until the interrupt is acknowledged by /IN SEL 0 or OUT SEL 0 via U36 driving the Reset pin on the flip flop. Typical output timing of U21 when speaking is a normally low signal that goes high for 74 microseconds, then low, with a repetition rate of 260 microseconds.

U18 output drives U36 (NAND gate C). This gate is enabled or disabled by BD INT EN 1 line (discussed above). When BD INT EN 1 is high, the output of U36 is enabled. U36 inverts the signal going through it.

External I/O

The external I/O is made up discrete parts and the circuit is duplicated 8 times. For the sake of this discussion we will describe the generic circuit using the same letter designators on the schematic.

These ports do not control anything on the speech board; the signal is merely routed through the speech board via D0 IN - D7 IN and D0 OUT - D7 OUT.

The INPUT/OUTPUT (INPUT) line is biased to 12 VDC by RB through CRA. When used as an input into the speech board, this line is pulled low externally through RA. This will cause the output of UA (LM239 comparator) to go high.

The INPUT/OUTPUT (OUTPUT) will turn on the QA transistor when Dx OUT is high. This will also pull the INPUT/OUTPUT line low. This will cause the output of UA to go high.

Relay

Relay K1 is mounted externally to the speech board. This is a 12 VDC relay with the coils connected across P1 pin 24 (TB11 pin 12) and P1 pin 25 (TB13 pin 1). The normally closed contact is across pins P1 21 (TB11 pin 9). The normally open contact is P1 pins 20 and 22 (TB11 pins 8, 10) which are connected together. The common relay contact is P1 pin 23 (TB11 pin 11).

Optical Coupler

The optical coupler protects all inputs external to the speech board. The optical coupler can provide up to 4400 VDC isolation between input and output.

An isolated input is applied to P1 pin 12 (TB9 pin 12) with a common for the isolated input on P1 pin 11 (TB9 pin 11). The collector output is connected to P1 pin 10 (TB9 pin 10) with the emitter connected to P1 pin 9 (TB9 pin 9). The collector needs a positive source of at least 5 volts. The emitter connector needs a resistive connection to the common for the collector connection.

The outputs will vary with the connections made to optical coupler. If transistor stage is configured as emitter follower, output taken from emitter when the input is high will give a high output. If the output is taken off the collector the signal is inverted and a high on the input will give a low on the output.

PART FOUR: SIGNAL DESCRIPTIONS

/BD IO RD	Enables data output from the speech board to the HBD bus.
/BD IO WR	Enables data input from the HBD bus.
/BD IO SEL	Selects the speech board for IO actions.
RT	Reset line from the HBD bus. Used to prevent false data on IO lines during a reset condition.
IN SEL 0	Resets /BD INT 1 board interrupt. Also enables output from speech encoder to HBD bus (not used).
IN SEL 1	Enables output from level detectors, squelch, and S3 status to the HBD bus.
IN SEL 2	Used to read in 8 bit general I/O port.

IN SEL 3	Used to read switch status of tenths and units switches.
IN SEL 4	Used to read switch status of tens and hundreds switches.
OUT SEL 0	Used to input speech data from HBD bus and resets /BD INT 1 board interrupt.
OUT SEL 1	Used to input control signals from HBD bus.
OUT SEL 2	Used to output to 8 bit general I/O port.
BD INT EN 1	Used to enable interrupts from speech board.
RCD/PB CNTRL	Used to select between speech decode or encode.
MUTE CNTRL	Used to mute speaker, does not affect radio signal.
AMP TEST	Used to test squelch detect circuit.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

Speech Board P1 Connector

NAME	CONNECTION	TERMINAL BLOCK
Speech Out	26	TB13-2
Speech Out	27	TB13-3
D0 I/O	1	TB9-1
D1 I/O	2	TB9-2
D2 I/O	3	TB9-3
D3 I/O	4	TB9-4
D4 I/O	5	TB9-5
D5 I/O	6	TB9-6
D6 I/O	7	TB9-7
D7 I/O	8	TB9-8
Opto Emitter	9	TB9-9
Opto Collector	10	TB9-10
+ Input	12	TB9-12
- Input	11	TB9-11
GND	29	TB13-5
GND	30	TB13-6
Relay Coil	25	TB13-1
Relay Coil	24	TB11-12
NO	20	TB11-8
NO	22	TB11-10
NC	21	TB11-9
COM	23	TB11-11
Squelch Input	28	TB13-4

The Servo Overlay board provides an interface between the Servo scanner and the Harmon Hot Box Detector. The Overlay board provides ± 200 volts to the scanner to power the bolometer. It also provides 160 VDC for model 7621 and 7707 sensors, and 24 VDC for 8808 and 8909 sensors.

The Servo Overlay board also provides an interface to the Servo ServoGraph chart recorder by providing a +180 Volt pen power supply and pen drive circuitry.

The output from the sensors is conditioned by the Servo overlay board before entering the Analog board on the HBD. Different settings are used on the board, depending on the model of Servo. A pot is provided to adjust the gain.

PART ONE: PHYSICAL DESCRIPTION

The Servo Overlay Board has connectors J1, J2, and J3, jumpers E2 to E5, and pots R3, R9, R44, R68, R85, R23, R27, R35 and R39.

Connector J1

The part of the printed circuit board which attaches to a cable labeled 'OVLY INTERFACE'. This cable is connected to the terminal blocks on the rear of the HBD cabinet. P1 has 50 gold-plated pins. The output voltages, sensor inputs, analog outputs, and pen drive signals are routed through this connector.

Connector J2

The part of the printed circuit board which slides into the connector on the motherboard in the HBD cabinet. P1 has 72 gold-plated contact pins. This connector only provides ± 12 volts and ground to the overlay board.

Connector J3

Pin type connector that provides the ± 200 volts output.

Jumpers E2-E5

Used to set the gain for different type of sensors.

Pot R3

Used to set the oscillator frequency of the PWM. The factory setting for the oscillator frequency is 25 kHz and should not be altered.

¹Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

Pot R44

Used to set the output level of the ± 200 volt power supply. This should be adjusted with no sensors connected and then readjusted after sensors are installed.

Pot R9

Used to set the output levels of the +160 volt supply and the 24 volt supply.

Pots R68 & R86

Used to set the heat output from the sensors as they interface into the HBD.

Pots R23 & R35

Used to set the Servo² chart recorder's gain.

Pots R27 & R39

Used to set the Servo chart recorder's zero level.

PART TWO: CIRCUIT DESCRIPTION

The Servo overlay board is divided into the following sections:

1. Pen drive
2. Switching power supply
 - a. ± 200 volts
 - b. + 160 volts
 - c. + 24 volts
 - d. +180 volts pen drive.
3. Sensor compensation circuit

Pen Drive Circuit

The inputs to the Servo pen drive come in on channel 1 (TB4-1) and channel 2 (TB4-4). The signal is then amplified by U2 LM224 op amp. The op amp drives Q7 & Q8 for channel 1 and Q9 & Q10 for channel 2 to provide the current necessary to drive the Servo chart recorder. The Servo chart recorder is connected to TB4-2 and TB4-3 for channel 1 and TB4-5 and TB4-6 for channel 2.

The gain is adjusted with R23 for channel 1 and R35 for channel 2. The damping adjustment is used to get the top of heat pulses as flat as possible. The gain must be reset after adjusting the damping pots (R27 for channel 1 and R39 for channel 2).

Switching Power Supply

The heart of the power supply is U1 an SG2526J pulse width modulator. This IC provides a drive output for the switching FETs in all of the power supplies. The outputs DR1 and DR2 are 180° out of phase, so that when one is on, the other is off.

²Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

The output oscillates at 25 kHz. This is controlled by R1, R2, R3 and C5. The output frequency can be adjusted via R3 but should not be reset in the field. This frequency is factory preset to give the best performance by the transformers (T1, T2, T3, T4).

± 200 Volt Power Supply

FETs Q12 and Q13 are driven by U1 as described above. The primary center tap of T4 is powered by Q11 (LAS-15U). Q11 regulates the 12 volt input down to 5 - 8.3 volts and is adjustable by means of R44. The step up voltage ratio across T4 is approximately 30:1 i.e. when the primary center tap reads 6.7 volts, the output is ± 200 volts.

FETs Q12 and Q13, when turned on, ground one end of T4's primary. When Q12 is on and Q13 is off, current flows between pins 1 and 2 on T4's primary. When a drive change occurs (every 40 μ sec), then Q12 is off and Q13 is on, and current flows between pins 2 and 3 on T4's primary.

T4 secondary pins 5 and 6 drive diode bridge rectifier CR37-CR40. These diodes in turn drive C36 and C38. The output is filtered to produce -200 volts. This output is between J3 pin 6 and J3 pin 4 (RTN). These are found on the back of the detector on TB2-12 and TB2-11 (RTN).

T4 secondary pins 7 and 8 drive diode bridge rectifier CR33-CR36. These diodes in turn drive C34 and C35. The output is filtered to produce +200 volts. This output is between J3 pin 1 and J3 pin 3 (RTN). These are found on the back of the detector on TB2-10 and TB2-11 (RTN).

+160 Volt Power Supply

FETs Q5 and Q6 are driven by U1 as described above. The primary center tap of T2 is powered by Q2 (LAS-15U). Q2 regulates the 12 volt input to 3.9 - 7.9 volts and is adjusted by R9. The adjustment range of the 160 volt supply is approximately 96 volts to 194 volts.

+24 Volt Power Supply

FETs Q5 and Q6 are driven by U1 as described above. The primary center tap of T3 is powered by Q2 (LAS-15U). Q2 regulates the 12 volt input to 3.9 - 7.9 volts and is adjusted by R9. The adjustment range of the 24 volt supply is approximately 12 volts to 24 volts.

+180 Volt Pen Power Supply

FETs Q3 and Q4 are driven by U1 as described above. The primary center tap of T1 is 8 volts powered by Q1 (LM217K). This is a fixed output regulator that supplies 8 volts.

Sensor Compensation Circuit

This circuit interfaces the various Servo³ sensors to the Harmon Analog board by amplifying the sensor output levels to the proper output level. The output of the Servo sensor is positive for older sensors using vacuum tubes and negative for newer sensors using transistor technology. Therefore, to get proper polarity to the Harmon Analog board, the following connections must be used.

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If the sensor is a transistor type, such as the Servo⁴ 8808 or the Servo 8909, the channel one input is hooked to TB2-2 and the channel one ground is hooked to TB2-1. The channel two signal is hooked to TB2-6, and the channel two ground is hooked to TB2-5.

If the sensor is a tube type, such as the Servo 7621 or the Servo 7707, the channel one input is hooked to TB2-1 and the channel one ground is hooked to TB2-2. The channel two signal is hooked to TB2-5, and the channel two ground is hooked to TB2-6.

Recommended Jumper Settings for Servo Sensors

Sensor	E2	E3	E4	E5
Servo 7621	open	open	1-2	1-2
Servo 7707	open	open	1-2	1-2
Servo 8808	1-2	1-2	open	open
Servo 8909	1-2	1-2	open	open
Servo 8909G	open	open	1-2	1-2

The output level is fine tuned with R68 for channel 1 and R84 for channel 2.

Channel 1 Description

The transistor output sensor (negative) feeds into TB2-2 and TB2-1 is connected to ground. The older sensor tube type (positive) feeds into TB2-1 and TB2-2 is connected to ground.

With the tube type sensor, the input is AC coupled and impedance matched into U3, an LM101A op amp. The gain setting of U3 is programmed by E2 and E4. For the tube type sensor, E4 should be shorted between pins 1 & 2 while E2 should be open. This will give the best gain results for a normal tube sensor. It is possible to adjust this gain by using different combinations of E2 and E4 jumpers. This might be necessary if a sun shield is used. Diodes CR41 & CR42 are used to surge protect the positive input of U3. The signal is amplified by U3 and not inverted.

With the newer type of sensor (transistor), the input is AC coupled and impedance matched into U3 (LM101A op amp). The gain setting of U3 is programmed by E2 and E4. For the transistor type sensor, E2 should be shorted between pins 1 & 2 while E4 should be open. This will give the best gain results for a normal transistor sensor. It is possible to adjust this gain by using different combinations of E2 and E4 jumpers. This might be necessary if a sun shield is used. The signal is inverted and amplified by U3.

The following applies to both the transistor and tube type sensor. The compensation module interfaces an ambient temperature sensor into the circuit to adjust the gain of the circuit with the change in ambient temperature. The compensation module is a voltage divider, with one

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leg as R6 and the other leg as R5, R4 and the ambient temperature sensor. As the resistance of the ambient temperature sensor decreases, the output voltage decreases; as the resistance increases, so does the output voltage.

The next stage is U2 which is an adjustable gain noninverting amplifier. The gain is adjusted through R68 to give a fine gain adjustment. The output is on J1 pin 17 and is connected to TB2-4 on the back of the HBD. The RTN line is J1 pin 22 and is connected to TB2-9 on the back of the HBD.

The amplifiers start to roll off (become low pass filters) at 200 Hz. This helps to filter out system noise.

Channel 2 Description

The transistor output sensor (negative) feeds into TB2-6 and TB2-5 is connected to ground. The older sensor tube type (positive) feeds into TB2-5 and TB2-6 is connected to ground.

With the tube type sensor, the input is AC coupled and impedance matched into U4 (LM101A OP amp). The gain setting of U3 is programmed by E3 and E5. For the tube type sensor, E5 should be shorted between pins 1 & 2 while E3 should be open. This will give the best gain results for a normal tube sensor. It is possible to adjust this gain by using different combinations of E3 and E5 jumpers. This might be necessary if a sun shield is used. The diodes CR45 & CR46 are used to surge protect the positive input of U4. The signal is amplified by U4 and not inverted.

With the newer type of sensor (transistor), the input is AC coupled and impedance matched into U4 (LM101A OP amp). The gain setting of U3 is programmed by E3 and E5. For the transistor type sensor, E3 should be shorted between pins 1 & 2 while E5 should be open. This will give the best gain results for a normal transistor sensor. It is possible to adjust this gain by using different combinations of E3 and E5 jumpers. This might be necessary if a sun shield is used. The signal is inverted and amplified by U4.

The following applies to both the transistor and tube type sensor. The compensation module interfaces an ambient temperature sensor into the circuit to adjust the gain of the circuit with the change in ambient temperature. The compensation module is a voltage divider, with one leg as R1 and the other leg as R2, R3 and the ambient temperature sensor. As the resistance of the ambient temperature sensor decreases, the output voltage decreases; as the resistance increases, so does the output voltage.

The next stage is U2 which is an adjustable gain noninverting amplifier. The gain is adjusted through R85 to give a fine gain adjustment. The output is on J1 pin 21 and is connected to TB2-8 on the back of the HBD. The RTN line is J1 pin 23 and is connected to TB2-9 on the back of the HBD.

The amplifiers start to roll off (become low pass filters) at 200 Hz. This helps to filter out system noise.

PART THREE: BOARD UPDATE

Caution: When working on a Servo⁵ Overlay board that has not been modified, turn the detector off and wait at least 3 minutes for the $\pm 200V$ supply to discharge before touching the board.

Changes

The following changes should have been made to the Servo Overlay board. These changes will provide a more stable ± 200 volt power supply.

Part Changes

CHANGE FROM	CHANGE TO
R42 10 Ω 5W	0 Ω SHORT
R43 1.5K	820 Ω 5%
R48 & R51 100K 1W	1K 1% 1/10W
R52 & R53 1M 1W	100K 1W

Additionally, the temperature sensor (HPN 226318-000) should be removed and replaced with two 10K resistors. Fish paper should also be added to the solder side of the board.

⁵Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

Servo⁶ Overlay J1 Connector

NAME	CONNECTION	TERMINAL BLOCK
160 VDC Out	1	TB4-7
160 VDC Return	2	TB4-8
12 - 24 VDC Out	3	TB4-9
12 - 24 VDC Return	4	TB4-10
Pen Input CH1	5	TB4-1
+ Chart Out CH1	6	TB4-2
- Chart Out CH1	7	TB4-3
Pen Input CH2	8	TB4-4
+ Chart Out CH2	9	TB4-5
- Chart Out CH2	10	TB4-6
+ CH1 Heat Input	14	TB2-1
- CH1 Heat Input	15	TB2-2
CH1 Ambient Temp	16	TB2-3
CH1 Out	17	TB2-4
GND	22	TB2-9
+ CH2 Heat Input	18	TB2-5
- CH2 Heat Input	19	TB2-6
CH2 Ambient Temp	20	TB2-7
CH2 Out	21	TB2-8
GND	23	TB2-9

Servo Overlay J3 Power Connector

NAME	CONNECTION	TERMINAL BLOCK
+200 VDC Out	1	TB2-10
200 VDC Return	3 & 4	TB2-11
-200 VDC Out	6	TB2-12

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The Time Date board interfaces to the Universal Processor board to provide a real time clock. This board also provides a serial link from the real time clock to the DCP3 board.

PART ONE: PHYSICAL DESCRIPTION OF BOARD

The Time Date board is a daughterboard that attaches to the Universal Processor board. It has connectors SD1, JA, and JB, and jumpers E1, E2, and E3.

Connector SD1

Connects the Time Date board to the Universal Processor board via a 36 pin connector.

Connector JA

Connects the Time Date board to the DCP3 board. This is a female right angle DB25 connector.

Connector JB

This connector is a female right angle DB25 connector. This connector is for future expansion and is not used at this time.

Jumper E1

Used to select or disable the board interrupt level. Interrupts are sent to the Universal Processor board via SD1.

Jumper E2

With the jumper removed, transfer of U9 & U4 RAM contents to EEPROM is disabled.
With the jumper installed, transfer of RAM contents to EEPROM is controlled by /STORE.

Jumper E3

With the jumper removed, transfer of U8 & U3 RAM contents to EEPROM is disabled.
With the jumper installed, transfer of RAM contents to EEPROM is controlled by /STORE.

PART TWO: CIRCUIT DESCRIPTION

The Time Date board is divided into the following sections:

1. Real time clock.
2. Communication interface.
3. Memory
4. Battery back up
5. Address decoding

Real Time Clock

The real time clock is U5, an MC146818. The real time clock provides a complete time of day clock and a 100 year calendar. The clock is battery backed up to maintain the proper time in case of power failure.

Crystal oscillator Y2 drives the clock at 32.768kHz, on pins 2 and 3.

Communication Interface

The communication interface is a Z8530, a serial communications controller (U14). The Z8530 can function as a serial to parallel/parallel to serial converter. It provides for dual-channel multi-protocol data communications.

The communication interface allows the DCP3 to interface to the real time clock on the Time Date board and communicate with the Universal Processor board. Although all communication between the Universal Processor and real time clock is performed on the 8 bit data bus, the DCP3 uses a serial channel (JA, through U16 and U17) into U14. U14 converts the serial to parallel to communicate with the Universal Processor board and the real time clock. For the real time clock and the Universal Processor board to communicate with the DCP3, U14 converts the parallel data to serial.

U16 1489A

A serial line receiver that interfaces serial channel A input signals into U14 (Z8530) on the Time Date board. The signals are data carrier detect (DCD), clear to send (CTS), recieved data (RxD), and the ring indicator (RI). These lines are connected through serial connector JA.

U17 1488A

A serial line driver that interfaces serial channel A output signals from U14 (Z8530) on the Time Date board to serial connector JA. JA is connected to the serial port on the DCP3. The signals are data term ready (DTR), request to send (RTS), and data transmitted (TxD).

U15 1489A

A serial line receiver that interfaces serial channel B input signals into U14 (Z8530) on the Time Date board. The signals are data carrier detect (DCD), clear to send (CTS), and recieved data (RxD). These lines are connected through serial connector JB.

U18 1488A

A serial line driver that interfaces serial channel B output signals from U14 (Z8530) on the Time Date board to serial connector JB. JB is reserved for future expansion and is not connected to any device.

Memory U3, U4, U8, U9

These nonvolatile 4 X 256 memories (X2212) store the alarm parameters of the HBD.

Chips U9 and U4 act together to make up an 8 bit byte, with U9 being the lower 4 bits. U4 and U9 are selected by /CS1.

Chips U8 and U3 act together to make up an 8 bit byte, with U8 being the lower 4 bits. U3 and U8 are selected by /CS2.

Battery Backup

The battery is a nickel-cadmium 3.6 volt rechargeable battery. The charge circuit consists of Q2, Q3, RT1, CR3, CR4, and bias resistors. Temperature sensor RT1 maintains the optimum charge current while compensating for variations in ambient temperature. The battery backup powers the real time clock in case of power failure.

Address Decoding

Address decoding is carried out by U7 (74HCT138), U11 (AND gate), U2 (OR gate), and U10 (NOR gate). The signals that drive the decoding originate on the Universal Processor board, and are introduced to this board via SD1.

PART THREE: SIGNAL DESCRIPTIONS

DB0-DB7	Bidirectional data lines from the Universal Processor board. They are interfaced to the Time Date board through SD1. These lines are also latched by U12 (74HCT373) to become A0-A7.
DBB0-DBB7	Derived from DB0-DB7 by U13 (74HCT245 octal transceiver). This allows the data to flow both directions under the control of pin 1 of U13. When pin 1 is high, data flow is from DB to DBB; when pin 1 is low, data flow is from DBB to DB. The data lines DBB0-DBB7 interface as data/address lines to U5 (MC146818 real time clock). They also interface as data lines to U14 (Z8530), and U3, U4, U8, U9 (X2212 memory).
BD-ALE	Latches U12 (74HCT373) to convert the DB0-DB7 data lines to address lines A0-A7. This signal is generated on the Universal Processor board and is interfaced to this board via SD1.
/BD_WR	Controls the write functions to U5 (real time clock), U14 (serial control interface), and U3, U4, U8, U9 (memory). This control is accomplished in conjunction with correct chip addressing and selection (see the memory I/O map). This signal is generated on the Universal Processor board and is interfaced via SD1 to this board.
/BD_RD	Combines with other signals to control read functions and data bus direction via U13. A detailed address break down is provided in the I/O memory map. This signal originates on the Universal Processor board and is interfaced via SD1 to this board.
/BD_DIR	Generated on the Universal Processor board and interfaced to the Time Date board via the SD1 connector. This line is used with /BD_RD and

/ISBX_SEL0 to control U13 (DB to DBB interface). When U13 pin 19 is low, data flows through U13; when high, isolation is provided (see I/O map).

/ISBX_SEL0

Generated on the Universal Processor board and interfaced to Time Date board via the SD1 connector. This line is used with /BD_RD and /BD_WR to control U13 (DB to DBB interface). When U13 pin 19 is low, data flows through U13; when high, isolation is provided. It is also used to help with the address decoding (see I/O map).

MPRO

Power up indicator from the Universal Processor board. MPRO is held low for 62 milliseconds upon power up to allow the circuits to stabilize. When low, turns off Q1 which keeps the +5 volt supply from reaching U10. This prevents accidental writes to U5 (real time clock), and memory (U3, U4, U8, U9).

/RT

Originates on the Universal Processor board and interfaced via SD1. Will reset the real time clock (U5) when low.

RXD

Originates on the Universal Processor board and interfaced via SD1. When high, selects channel A on U14 (control interface) for read and writes. When low, selects channel B on U14 (control interface) for read and writes.

MEM+

Battery back up power. When system power is present, this voltage is supplied by Q2 & Q3 which derive the power from +5 volts. This voltage also keeps the nicad battery charged. RT1 regulates the current to the battery with changes in temperature to give the correct charge rate. When system power is unavailable, the real time clock (U5) is kept powered up from the battery via RT1, CR3, and R20.

/STORE

When low, initiates the transfer of the entire contents of RAM into the EEPROM. Note that when jumpers E2 and E3 are open, the store operation is disabled. This signal is generated on the Time Date board by address decoding performed by U7 (74HCT138 3 to 8 multiplexer), U11 (AND gate), U1, and U10 (NOR gates). See I/O memory map for equation.

/RECALL

When low, initiates the transfer of the entire contents of EEPROM into RAM. The /RECALL line is controlled by U7 (74HCT138 multiplexer) and U11 (AND gate). See I/O memory map for equation.

/CS2

When low, memory chips U3 & U8 are selected for read or write operations. The /SC2 line is controlled by U7 (74HCT138 3 to 8 multiplexer) and U11 (AND gate). See I/O memory map for equation.

- /CS1** When low, memory chips U4 & U9 are selected for read or write operations. The /SC2 line is controlled by U7 (74HCT138 3 to 8 multiplexer) and U11 (AND gate). See I/O memory map for equation.
- /INTACK** Interrupt acknowledge, generated on the Time Date board by the address decoding logic. This line, when low, tells the Z8530 (U14) that the system has acknowledged an interrupt generated by it. The /INTACK line is controlled by U7 (74HCT138) and U11. See I/O memory map for equation.
- /CE** This is the chip select for U14 (Z8531). When low, this line enables reads and writes to this chip. The /CE line is controlled by U7 and U11 (see I/O memory map for equation).

U5 MC146818 Signal Lines

AD0-AD7 (pins 4-11) are bidirectional input lines. They provide both the address and data lines depending on the state of the chip select lines. The address must be valid on AD0-AD5 prior to the fall of DS. There are 64 bytes total: 50 general purpose bytes, 10 RAM bytes that contain the time, calendar, and alarm data, and 4 control and status bytes. See table below for map information.

Either the /RD (pin 17) line or the DS line, when low, selects U5 (real time clock) for output enable. This is typically used during a read operation. This line is selected by U2 (OR gate), U6 & U11 (AND gates), and U7 (3 to 8 Multiplexer). See I/O memory map for address decoder details.

The /CE (pin 13) chip enable line must be low in order to read or write to U5. This line is generated by /RT through U10 (NOR gate).

When a positive going pulse is present on the AS (pin 14) address strobe line, it demultiplexes the real time clock internal bus. When a low going pulse is present, it causes address to latched internal on U5 bus. This signal is generated by U10 (NOR gate) U7 (3 to 8 multiplexer) and U11 (AND gate). See I/O map for address decoding information.

When the /WR line (pin 15) is high and the chip is selected, a read cycle is executed on the real time clock. When /WR is low and the chip is selected, a write cycle is generated by the real time clock. This signal is generated by U2 (OR gate), U7 (3 to 8 multiplexer), and U11 (AND gate). See I/O map for address decoding information.

/IRQ (pin 19) is pulled low by the MC146818 and will remain low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is present. To clear the /IRQ, read register C. This line drives U6 (AND gate), U1, U10 (NOR gates). Jumper E1 determines interrupt level - either /BD_INT_0, /BD_INT_1, or disabled if the jumper is not installed.

CK OUT (pin 21) carries the same frequency clock as at pins 2 & 3.

CKFS (pin 20) sets the divide rate for CK OUT. When it is tied high, CK OUT has the same frequency clock as pins 2 & 3.

/RESET (pin 18) clears alarms and the periodic interrupt enable when low. This line is pulled low by /RT which originates on the Universal Processor board.

The PS (pin 22) power sense input is held low during power up to indicate the RAM data is unstable. When the power is stable the pin will go high.

U14 Z8530 Signal Lines

- /INT** The Z8530 pulls this line low to request an interrupt. This line interfaces through U6 (AND gate) and is then inverted through U1 and again through U10. The interrupt setting is made with jumper E1. A jumper between A & B selects /BD_INT_0. A jumper between B & C selects /BD_INT_1. Removing the jumper disables the interrupt from reaching the Universal processor board.
- PCLK** This is the master clock used to synchronize all internal signals of the Z8530. It is generated by Y1 (4.0MHz) and U1.
- /CE** Selects U5 for a read or write operation. This signal is generated by U7 (3 to 8 multiplexer) and U11 (AND gate). See the I/O memory map for address information.
- /WR** When this line is low and U14 is selected a write operation will be performed by U14 (Z8530). This line is generated by U19 (OR gate) and U11 (AND gate). The /BD-WR signal that drives U11 originates on the Universal Processor board. See I/O memory map for address information.
- /RS** When this line is low and U14 is selected a read operation will be performed by U14 (Z8530). This line is generated by U11 (AND gate) by logically ANDing /BD-RD and /RT. See I/O memory map for address information.
- /DCDA** Channel A data carrier detect. When a logic low is detected an interrupt will be generated via the /INT line. This signal is passed through U16 (1489A line receiver).
- /CTSA** Channel A clear to send line. When /CTSA is pulled low the data transmitters are enabled. This signal is passed through U16 (1489A line receiver).
- RXDA** Channel A serial data input line from DCP3 to U14. This signal is passed through U16 (1489A line receiver).

/RIA	Channel A ring indicator line. When low, it causes U14 to set the internal ring indicator bit. This signal is passed through U16 (1489A line receiver).
/DTRA	Channel A data terminal ready bit, low when channel A is ready to send. This signal is passed through U17 (1488 line transmitter).
/RTSA	Channel A Request To Send bit. Is low when the request to send bit is set in the write register. This signal is passed through U17 (1488 line transmitter).
/TXDA	Channel A transmit data, serial data output channel A from U14 to DCP3. This signal is passed through U17 (1488 line transmitter).
/DCDB	Channel B data carrier detect. When a logic low is detected an interrupt will be generated via the /INT line. This signal is passed through U15 (1489 line receiver).
/CTSB	Channel B clear to send line when pulled low enables the data transmitters. This signal is passed through U15 (1489 line receiver).
RXDB	Channel B serial data input line. This signal is passed through U15 (1489 line receiver).
/DTRB	Channel A data terminal ready bit, low when channel B ready to send. This signal is passed through U18 (1488 line transmitter).
/RTSB	Channel B Request To Send bit active low. Is low when request to send bit is set in the write register. This signal is passed through U18 (1488 line transmitter).
/TXDB	Channel B transmit data, serial data output channel B. This signal is passed through U18 (1488 line transmitter).

JA Signal Descriptions

Data Carrier Detect (JA pin 8)

Channel A data carrier detect. When a logic low is detected it signals the presence of a carrier. It is generated on the DCP3 board. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Clear to Send (JA pin 5)

Channel A clear to send. When pulled low it signals that the DCP3 is ready to receive data and that U14 can send the data. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Received Data (JA pin 3)

Channel A serial data input line, from DCP3. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Ring Indicator (JA pin 22)

Channel A ring indicator line. When low, a ring is indicated by the DCP3. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Data Term Ready (JA pin 20)

Channel A data terminal ready line. Low when U14 is ready to send data to the DCP3. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

Request to Send (JA pin 4)

Channel A Request To Send line. Is low when request to send bit is set in the write register of U14. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

Data Transmit (JA pin 2)

Channel A transmit data, serial data output channel A to the DCP3. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

JB Signal Descriptions

Note: The JB connector is reserved for future expansion and is not connected on current production model Time Date boards.

Data Carrier Detect (JB pin 8)

Channel B data carrier detect. When a logic low is detected it signals the presence of a carrier. It is generated on the DCP3 board. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Clear to Send (JB pin 5)

Channel B clear to send. When pulled low it signals that the DCP3 is ready to receive data and that U14 can send the data. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Received Data (JB pin 3)

Channel B serial data input line, from DCP3. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Data Term Ready (JB pin 20)

Channel A data terminal ready line. Low when U14 is ready to send data to the DCP3. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

Request to Send (JB pin 4)

Channel A Request To Send line. Is low when request to send bit is set in the write register of U14. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

Data Transmit (JB pin 2)

Channel A transmit data, serial data output channel A to the DCP3. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

U13 Transceiver Signal Descriptions

/E pin 19

When low, data flows through U13 (74HCT245 transceiver). When high, U13 provides isolation between the DB and DBB data busses. The signal is developed through U6 (AND gates) and U2 (OR gates).

DR pin 1

When high, data flows from the Universal Processor to the Time Date board. When low, data flows from the Time Date board to the Universal Processor board. The signal is generated by U2 (OR gate).

Connects the Time Date board to the Universal Processor board via a 36 pin connector.

Connector JA

Connects the Time Date board to the DCP3 board. This is a female right angle DB25 connector.

Connector JB

This connector is a female right angle DB25 connector. This connector is for future expansion and is not used at this time.

Jumper E1

Used to select or disable the board interrupt level. Interrupts are sent to the Universal Processor board via SD1.

Jumper E2

With the jumper removed, transfer of U9 & U4 RAM contents to EEPROM is disabled.
With the jumper installed, transfer of RAM contents to EEPROM is controlled by /STORE.

Jumper E3

With the jumper removed, transfer of U8 & U3 RAM contents to EEPROM is disabled.
With the jumper installed, transfer of RAM contents to EEPROM is controlled by /STORE.

PART TWO: CIRCUIT DESCRIPTION

The Time Date board is divided into the following sections:

1. Real time clock.
2. Communication interface.
3. Memory
4. Battery back up
5. Address decoding

Real time clock

The real time clock is U5, an MC146818. The real time clock provides a complete time of day clock and a 100 year calendar. The clock is battery backed up to maintain the proper time in case of power failure.

Crystal oscillator Y2 drives the clock at 32.768kHz, on pins 2 and 3.

Communication Interface

The communication interface is a Z8530, a serial communications controller (U14). The Z8530 can function as a serial to parallel/parallel to serial converter. It provides for dual-channel multi-protocol data communications.

The communication interface allows the DCP3 to interface to the real time clock on the Time Date board and communicate with the Universal Processor board. Although all communication between the Universal Processor and real time clock is performed on the 8 bit data bus, the DCP3 uses a serial channel (JA, through U16 and U17) into U14. U14 converts the serial to parallel to communicate with the Universal Processor board and the real time clock. For the real time clock and the Universal Processor board to communicate with the DCP3, U14 converts the parallel data to serial.

U16 1489A

A serial line receiver that interfaces serial channel A input signals into U14 (Z8530) on the Time Date board. The signals are data carrier detect (DCD), clear to send (CTS), recieved data (RxD), and the ring indicator (RI). These lines are connected through serial connector JA.

U17 1488A

A serial line driver that interfaces serial channel A output signals from U14 (Z8530) on the Time Date board to serial connector JA. JA is connected to the serial port on the DCP3. The signals are data term ready (DTR), request to send (RTS), and data transmitted (TxD).

U15 1489A

A serial line receiver that interfaces serial channel B input signals into U14 (Z8530) on the Time Date board. The signals are data carrier detect (DCD), clear to send (CTS), and recieved data (RxD). These lines are connected through serial connector JB.

U18 1488A

A serial line driver that interfaces serial channel B output signals from U14 (Z8530) on the Time Date board to serial connector JB. JB is reserved for future expansion and is not connected to any device.

Memory U3, U4, U8, U9

These nonvolatile 4 X 256 memories (X2212) store the alarm parameters of the HBD.

Chips U9 and U4 act together to make up an 8 bit byte, with U9 being the lower 4 bits. U4 and U9 are selected by /CS1.

Chips U8 and U3 act together to make up an 8 bit byte, with U8 being the lower 4 bits. U3 and U8 are selected by /CS2.

Battery Backup

The battery is a nickel-cadmium 3.6 volt rechargeable battery. The charge circuit consists of Q2, Q3, RT1, CR3, CR4, and bias resistors. Temperature sensor RT1 maintains the optimum charge current while compensating for variations in ambient temperature. The battery backup powers the real time clock in case of power failure.

Address Decoding

Address decoding is carried out by U7 (74HCT138), U11 (AND gate), U2 (OR gate), and U10 (NOR gate). The signals that drive the decoding originate on the Universal Processor board, and are introduced to this board via SD1.

PART THREE: SIGNAL DESCRIPTIONS

DB0-DB7	Bidirectional data lines from the Universal Processor board. They are interfaced to the Time Date board through SD1. These lines are also latched by U12 (74HCT373) to become A0-A7.
DBB0-DBB7	Derived from DB0-DB7 by U13 (74HCT245 octal transceiver). This allows the data to flow both directions under the control of pin 1 of U13. When pin 1 is high, data flow is from DB to DBB; when pin 1 is low, data flow is from DBB to DB. The data lines DBB0-DBB7 interface as data/address lines to U5 (MC146818 real time clock). They also interface as data lines to U14 (Z8530), and U3, U4, U8, U9 (X2212 memory).
BD-ALE	Latches U12 (74HCT373) to convert the DB0-DB7 data lines to address lines A0-A7. This signal is generated on the Universal Processor board and is interfaced to this board via SD1.
/BD_WR	Controls the write functions to U5 (real time clock), U14 (serial control interface), and U3, U4, U8, U9 (memory). This control is

accomplished in conjunction with correct chip addressing and selection (see the memory I/O map). This signal is generated on the Universal Processor board and is interfaced via SD1 to this board.

/BD_RD Combines with other signals to control read functions and data bus direction via U13. A detailed address break down is provided in the I/O memory map. This signal originates on the Universal Processor board and is interfaced via SD1 to this board.

/BD_DIR Generated on the Universal Processor board and interfaced to the Time Date board via the SD1 connector. This line is used with /BD_RD and /ISBX_SELO to control U13 (DB to DBB interface). When U13 pin 19 is low, data flows through U13; when high, isolation is provided (see I/O map).

/ISBX_SELO Generated on the Universal Processor board and interfaced to Time Date board via the SD1 connector. This line is used with /BD_RD and /BD_WR to control U13 (DB to DBB interface). When U13 pin 19 is low, data flows through U13; when high, isolation is provided. It is also used to help with the address decoding (see I/O map).

MPRO Power up indicator from the Universal Processor board. MPRO is held low for 62 milliseconds upon power up to allow the circuits to stabilize. When low, turns off Q1 which keeps the +5 volt supply from reaching U10. This prevents accidental writes to U5 (real time clock), and memory (U3, U4, U8, U9).

/RT Originates on the Universal Processor board and interfaced via SD1. Will reset the real time clock (U5) when low.

RXD Originates on the Universal Processor board and interfaced via SD1. When high, selects channel A on U14 (control interface) for read and writes. When low, selects channel B on U14 (control interface) for read and writes.

MEM+ Battery back up power. When system power is present, this voltage is supplied by Q2 & Q3 which derive the power from +5 volts. This voltage also keeps the nicad battery charged. RT1 regulates the current to the battery with changes in temperature to give the correct charge rate. When system power is unavailable, the real time clock (U5) is kept powered up from the battery via RT1, CR3, and R20.

/STORE When low, initiates the transfer of the entire contents of RAM into the EEPROM. Note that when jumpers E2 and E3 are open, the store operation is disabled. This signal is generated on the Time Date board

by address decoding performed by U7 (74HCT138 3 to 8 multiplexer), U11 (AND gate), U1, and U10 (NOR gates). See I/O memory map for equation.

- /RECALL** When low, initiates the transfer of the entire contents of EEPROM into RAM. The /RECALL line is controlled by U7 (74HCT138 multiplexer) and U11 (AND gate). See I/O memory map for equation.
- /CS2** When low, memory chips U3 & U8 are selected for read or write operations. The /SC2 line is controlled by U7 (74HCT138 3 to 8 multiplexer) and U11 (AND gate). See I/O memory map for equation.
- /CS1** When low, memory chips U4 & U9 are selected for read or write operations. The /SC2 line is controlled by U7 (74HCT138 3 to 8 multiplexer) and U11 (AND gate). See I/O memory map for equation.
- /INTACK** Interrupt acknowledge, generated on the Time Date board by the address decoding logic. This line, when low, tells the Z8530 (U14) that the system has acknowledged an interrupt generated by it. The /INTACK line is controlled by U7 (74HCT138) and U11. See I/O memory map for equation.
- /CE** This is the chip select for U14 (Z8531). When low, this line enables reads and writes to this chip. The /CE line is controlled by U7 and U11 (see I/O memory map for equation).

U5 MC146818 Signal Lines

AD0-AD7 (pins 4-11) are bidirectional input lines. They provide both the address and data lines depending on the state of the chip select lines. The address must be valid on AD0-AD5 prior to the fall of DS. There are 64 bytes total: 50 general purpose bytes, 10 RAM bytes that contain the time, calendar, and alarm data, and 4 control and status bytes. See table below for map information.

Either the /RD (pin 17) line or the DS line, when low, selects U5 (real time clock) for output enable. This is typically used during a read operation. This line is selected by U2 (OR gate), U6 & U11 (AND gates), and U7 (3 to 8 Multiplexer). See I/O memory map for address decoder details.

The /CE (pin 13) chip enable line must be low in order to read or write to U5. This line is generated by /RT through U10 (NOR gate).

When a positive going pulse is present on the AS (pin 14) address strobe line, it demultiplexes the real time clock internal bus. When a low going pulse is present, it causes address to latched internal on U5 bus. This signal is generated by U10 (NOR gate) U7 (3 to

8 multiplexer) and U11 (AND gate). See I/O map for address decoding information.

When the /WR line (pin 15) is high and the chip is selected, a read cycle is executed on the real time clock. When /WR is low and the chip is selected, a write cycle is generated by the real time clock. This signal is generated by U2 (OR gate), U7 (3 to 8 multiplexer), and U11 (AND gate). See I/O map for address decoding information.

/IRQ (pin 19) is pulled low by the MC146818 and will remain low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is present. To clear the /IRQ, read register C. This line drives U6 (AND gate), U1, U10 (NOR gates). Jumper E1 determines interrupt level - either /BD_INT_0, /BD_INT_1, or disabled if the jumper is not installed.

CK OUT (pin 21) carries the same frequency clock as at pins 2 & 3.

CKFS (pin 20) sets the divide rate for CK OUT. When it is tied high, CK OUT has the same frequency clock as pins 2 & 3.

/RESET (pin 18) clears alarms and the periodic interrupt enable when low. This line is pulled low by /RT which originates on the Universal Processor board.

The PS (pin 22) power sense input is held low during power up to indicate the RAM data is unstable. When the power is stable the pin will go high.

U14 Z8530 Signal Lines

/INT The Z8530 pulls this line low to request an interrupt. This line interfaces through U6 (AND gate) and is then inverted through U1 and again through U10. The interrupt setting is made with jumper E1. A jumper between A & B selects /BD_INT_0. A jumper between B & C selects /BD_INT_1. Removing the jumper disables the interrupt from reaching the Universal processor board.

PCLK This is the master clock used to synchronize all internal signals of the Z8530. It is generated by Y1 (4.0MHz) and U1.

/CE Selects U5 for a read or write operation. This signal is generated by U7 (3 to 8 multiplexer) and U11 (AND gate). See the I/O memory map for address information.

/WR When this line is low and U14 is selected a write operation will be performed by U14 (Z8530). This line is generated by U19 (OR gate) and U11 (AND gate). The /BD-WR signal that drives U11 originates on the Universal Processor board. See I/O memory map for address information.

/RS	When this line is low and U14 is selected a read operation will be performed by U14 (Z8530). This line is generated by U11 (AND gate) by logically ANDing /BD-RD and /RT. See I/O memory map for address information.
/DCDA	Channel A data carrier detect. When a logic low is detected an interrupt will be generated via the /INT line. This signal is passed through U16 (1489A line receiver).
/CTSA	Channel A clear to send line. When /CTSA is pulled low the data transmitters are enabled. This signal is passed through U16 (1489A line receiver).
RXDA	Channel A serial data input line from DCP3 to U14. This signal is passed through U16 (1489A line receiver).
/RIA	Channel A ring indicator line. When low, it causes U14 to set the internal ring indicator bit. This signal is passed through U16 (1489A line receiver).
/DTRA	Channel A data terminal ready bit, low when channel A is ready to send. This signal is passed through U17 (1488 line transmitter).
/RTSA	Channel A Request To Send bit. Is low when the request to send bit is set in the write register. This signal is passed through U17 (1488 line transmitter).
/TXDA	Channel A transmit data, serial data output channel A from U14 to DCP3. This signal is passed through U17 (1488 line transmitter).
/DCDB	Channel B data carrier detect. When a logic low is detected an interrupt will be generated via the /INT line. This signal is passed through U15 (1489 line receiver).
/CTSB	Channel B clear to send line when pulled low enables the data transmitters. This signal is passed through U15 (1489 line receiver).
RXDB	Channel B serial data input line. This signal is passed through U15 (1489 line receiver).
/DTRB	Channel B data terminal ready bit, low when channel B ready to send. This signal is passed through U18 (1488 line transmitter).
/RTSB	Channel B Request To Send bit active low. Is low when request to send bit is set in the write register. This signal is passed through U18 (1488 line transmitter).
/TXDB	Channel B transmit data, serial data output channel B. This signal is passed through U18 (1488 line transmitter).

JA Signal Descriptions

Data Carrier Detect (JA pin 8)

Channel A data carrier detect. When a logic low is detected it signals the presence of a carrier. It is generated on the DCP3 board. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Clear to Send (JA pin 5)

Channel A clear to send. When pulled low it signals that the DCP3 is ready to receive data and that U14 can send the data. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Received Data (JA pin 3)

Channel A serial data input line, from DCP3. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Ring Indicator (JA pin 22)

Channel A ring indicator line. When low, a ring is indicated by the DCP3. It is passed through U16 (1489 line receiver) to U14 (Z8530).

Data Term Ready (JA pin 20)

Channel A data terminal ready line. Low when U14 is ready to send data to the DCP3. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

Request to Send (JA pin 4)

Channel A Request To Send line. Is low when request to send bit is set in the write register of U14. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

Data Transmit (JA pin 2)

Channel A transmit data, serial data output channel A to the DCP3. It is passed from U14 (Z8530) through U17 (1488 line transmitter).

JB Signal Descriptions

Note: The JB connector is reserved for future expansion and is not connected on current production model Time Date boards.

Data Carrier Detect (JB pin 8)

Channel B data carrier detect. When a logic low is detected it signals the presence of a carrier. It is generated on the DCP3 board. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Clear to Send (JB pin 5)

Channel B clear to send. When pulled low it signals that the DCP3 is ready to receive data and that U14 can send the data. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Received Data (JB pin 3)

Channel B serial data input line, from DCP3. It is passed through U15 (1489 line receiver) to U14 (Z8530).

Data Term Ready (JB pin 20)

Channel A data terminal ready line. Low when U14 is ready to send data to the DCP3. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

Request to Send (JB pin 4)

Channel A Request To Send line. Is low when request to send bit is set in the write register of U14. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

Data Transmit (JB pin 2)

Channel A transmit data, serial data output channel A to the DCP3. It is passed from U14 (Z8530) through U18 (1488 line transmitter).

U13 Transceiver Signal Descriptions

/E pin 19

When low, data flows through U13 (74HCT245 transceiver). When high, U13 provides isolation between the DB and DBB data busses. The signal is developed through U6 (AND gates) and U2 (OR gates).

DR pin 1

When high, data flows from the Universal Processor to the Time Date board. When low, data flows from the Time Date board to the Universal Processor board. The signal is generated by U2 (OR gate).

Note: All designators for the original Analog I board are shown in braces '{}'. All other designators should be assumed to refer to Analog II board components.

The Analog Board interfaces the analog sensors to the digital portion of the Hot Box Detector. The alarm settings can be set on this board for the HBD. The Analog board can either be a hot bearing detector or a hot wheel detector, depending on jumper settings. A HBD can have 1 each hot bearing and hot wheel detector.

The Analog board interfaces either the IRIS or model 38 scanners to the CPU inside the HBD. When a Servo⁷ IR sensor is used, it is interfaced through the Servo Overlay board to the Analog board. When using a Model 38 or IRIS, the Servo Overlay board is not used, and the sensor interfaces directly to the Analog board. The Analog board scales and takes a peak heat reading, then digitizes the peak heat reading for each bearing with an A/D converter.

The Analog board converts the single sine wave from both gate and advance wheel pickup transducers into interrupts and bit values that are fed to the Universal Processor board.

The Analog board interfaces an ambient temperature sensor to the Universal Processor board. The input from the temperature sensor is scaled and digitized.

The Analog board converts the digital signals from the Universal Processor board to Analog signals to drive the chart recorder. It also converts the self test signals from the Universal Processor board.

Extensive self tests are performed on the Analog board to verify that it remains fully operational.

PART ONE: PHYSICAL DESCRIPTION

The Analog board has connectors P1, P2, header blocks P3 and P4, plug in modules IN1 - IN5, and 6 alarm pots.

Connector P1

The part of the printed circuit board which attaches to a cable labeled 'HBD ANALOG'. This cable is connected to the terminal blocks on the rear of the HBD cabinet. P1 has 56 gold-plated pins. This connector interfaces the analog signals into and out of the analog board.

⁷Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

Connector P2

The part of the printed circuit board which slides into the connector on the motherboard in the HBD cabinet. P1 has 72 gold-plated contact pins. All power, interrupts, data, and address lines pass through this connector.

Header P3 {BD INT SEL}

Sets the interrupt level from the analog board to the Universal Processor board via P2. The setting for a hot bearing board is typically 3, while the jumper is removed for a hot wheel board.

Header P4 {BOARD IO SEL}

Sets the I/O select from the analog board to the Universal Processor board via P2. The setting for a Hot bearing board is typically 4, while the jumper is normally set to 5 for a hot wheel board.

IN1

Input network IN1 is to impedance match the wheel gate pickups. It is inserted into an 8 pin dip socket. Pins 1 and 8 load wheel pickup A while pins 4 and 5 load wheel pickup B.

IN2

Input network IN2 is to impedance match the advance wheel pickups. It is inserted into an 8 pin dip socket. Pins 1 and 8 load advance pickup A while pins 4 and 5 load advance pickup B.

IN3

Input network IN3 is to interface the ambient temperature sensor into the analog board.

IN4

Input network IN4 is used to interface with auxiliary analog inputs, such as a weather station.

IN5

Input network IN5 is used to scale and impedance match the various IR sensors into the Analog board. Some networks have a pot adjustment for each channel allowing an adjustment range of ± 2 mm when an input of 15 mm is applied. The input network must be the correct one to scale the sensor for valid heat readings. Note that the system cannot detect an improper IN5 network - the only way to do so is to check the system using a calibrated heat source.

R28 {R116A}

10K pot used as a voltage divider tied between +5 volts and ground. This is used to set the minimum level for single axle alarm. This setting can be overridden by the DCP3.

R29 {R116B} Is a 10K pot used as a voltage divider tied between +5 volts and ground. This is used to adjust the absolute alarm Hi limit. This setting can be overridden by the DCP3.

R30 {R122C}

10K pot used as a voltage divider tied between +5 volts and ground. This is used to adjust car side slope. This is a number which represents a specific slope line selection from the car side analysis graph. This setting can be overridden by the DCP3.

R31 {R122D}

10K pot used as a voltage divider tied between +5 volts and ground. This is used to adjust car side slope limit. The number represents a specific graph selection from the group of car side analysis graphs. This setting can be overridden by the DCP3.

R32 {R123E}

10K pot used as a voltage divider tied between +5 volts and ground. This is used to adjust the distance between the centers of the gate transducers, in inches.

R33 {R123F}

10K pot used as a voltage divider tied between +5 volts and ground. Sets minimum level of hot wheel alarm (if used as a hot wheel detector).

PART TWO: CIRCUIT DESCRIPTION

The analog board can be divided into the following sections:

1. Gating transducer interface.
2. Advance transducer interface.
3. IN5 interface module
4. IN4 interface module
5. IN3 interface module
6. 16 channel analog multiplexer, and control logic
7. Peak hold circuit and control logic.
 - a. Input heat from IN5
 - b. Test signals
 - c. Power supply monitoring signals
8. DACs
9. Chart recorder drive
10. DAC routing, and control
11. DAC generated test signals
12. A/D converter, and buffer.
13. Digital output buffers
14. Digital input buffers
15. Address decoding

Gating Transducer Interface.

Note: Only channel A will be discussed here, as channel B operates identically except for the reference designators and output bits. The designators for channel B can be obtained from the schematic.

The input from the wheel transducer is a single sine wave. The zero crossing occurs when the wheel is centered over the transducer.

The input is a differential input through a network of four 4.7K resistors R35 - R36 {R3 - R6}. This balancing network is primarily used to balance electric rail current to cancel out the traction current. The input header IN1 is used to correctly load the wheel pickup. When using a Harmon wheel pickup, this value is 10 K Ω . The bidirectional transzors D12, D13 are set to shunt transients higher than 7.5 volts to ground. The wheel pickups typically output 2 to 3 volts peak. {The Analog I uses silicone diodes tied to ± 6 volts for transient protection. The diodes start to clamp off transients at 6.7 volts. The diodes are CR3 - CR6.} Capacitors C35 to C38, {C3, C4, C11, C60} form a low pass circuit turned to approximately 50 HZ to help filter out noise without affecting the output level from high speed trains.

The difference amplifier IC21A {U1A} amplifies the input 2 times and produces a single ended output. The signal is then wave shaped to be a ± 1.5 volt peak square wave by diodes D14, D34, D36, D37 {CR27-CR30}.

The square wave is then run through a positive and a negative comparator.

Positive Comparator

IC25B {U3A} has a normally high output. The reference (positive pin) is biased at .4 VDC when the output is high. The .4 VDC reference is developed by R48-R50 {R59-R61} voltage divider. R48 {R61} is a positive feed back for hysteresis. When the input increases to more than .4 volts the output goes low. Due to hysteresis the output will remain low until the input drops below .2 volts. The reference pin voltage will change to .2 VDC when the output is low.

The comparator output goes through IC24D {U7D}, a 74HC086 exclusive OR gate. The output of the exclusive OR is controlled by P31. P31 is normally high when waiting for a positive wheel gate. This enables the signal to flow through IC24D {U7D}. This activates interrupt line /BDINT through IC23A {U6A}. This line is enabled by P30 being high. The output status of comparator IC23A {U6A} is available on P00 (data bus). The Universal Processor board acknowledges this interrupt by driving P30 low, disabling this interrupt. P31 is pulled low when the interrupt is acknowledged by the Universal Processor board.

Negative Comparator

IC22B {U3B} is normally a low output. The reference input (positive input) is biased at -.45 volts. The -.45 VDC reference is developed by R46 and R62 {R63 and R68}. When the input becomes more negative than -.45 volts, the output goes high. The output remains high

until the input becomes more positive than the -.45 volts. The output goes through IC23C {U6C} (NAND gate) to become /BDINT, the interrupt line.

The capability of IC23C {U6C} to generate an interrupt is controlled through software. Line P32 must be high in order for IC23C {U6C} to generate an interrupt. P32 is normally low and is high after the positive comparator has tripped. P32 is controlled by Dout data bus bit 3. The output status of comparator IC23C {U6C} is always available as P01 on the data bus.

Advance Transducer Interface.

Note: Since the advance transducer channels operate identically except for the reference designators and output bits, only channel A will be covered. The designators for channel B can be obtained from the schematic.

The input from the wheel transducer is a single sine wave. The zero crossing occurs when the wheel is centered over the transducer.

The input is a differential input through a network of four 4.7K resistors R67 - R70 {R11 - R14}. This balancing network is primarily used to balance electric rail current to cancel out the traction current. The input header IN2 is used to correctly load the wheel pickup. When using a Harmon wheel pickup, this value is 10 K Ω . The bidirectional transzorb D18, D19 are set to shut transients higher than 7.5 volts to ground. The wheel pickups typically put out 2 to 3 volts peak. {The analog 1 uses silicone diodes to $\pm$ 6 volts for transient protection. The diodes start to clamp off transients at 6.7 volts. The diodes are (CR11 - CR14).} Capacitors C45 to C47 {C7, C8, C15} form a low pass circuit turned to approximately 50 HZ to help filter out noise without affecting the output level from high speed trains.

The sine wave is run through a negative comparator. The comparator IC26A {U2A} has a normally low output. The reference (positive pin) is biased at -.24 VDC. When the input becomes more negative than -.24 volts, the output goes high. The output remains high until the input becomes more positive than -.34 volts. This is due to the hysteresis from R74 {R61}.

The comparator output goes through IC24A {U7A}, a 74HC086 exclusive OR gate. The output of the exclusive OR is controlled by P41. P41 is normally low, enabling the signal to flow through IC24A {U7A}.

The signal then fires the /BDINT through IC27D {U8D}. This line is enabled by P40 being high. The Universal Processor board acknowledges this interrupt by driving P40 low, disabling this interrupt. The output of IC24A {U7A} can still be read through P04.

Interface Module IN5

The type of interface module depends on the IR sensor being interfaced to. There are three main types of IR sensors. These are the Harmon Electronics Model 38 and IRIS, and all types of Servo scanners.

The -000 Harmon standard network is used with a model 38 preamp. The IN5 module has four resistors (2 per channel) 26.7K and 10K. These resistors scale down the signal to 27% of its original value.

The .1 μ F capacitors bypass high frequency noise off the input line for each channel. The 1 μ F coupling capacitor AC couples the heat reading to the analog board. The 1.5KE7.5C bidirectional transzorbs shunt transients greater than 7.5 volts to ground.

The -001 net work works with Servo⁸ overlays and IRIS. The IN5 module has four resistors (2 per channel) 39K and 1M. These resistors scale down the signal to 96% of its original value. The 1 μ F coupling capacitor AC couples the heat reading to the analog board. The transients greater than 7.5 volts are shunted to ground by back to back zener diodes 1N5235B.

The -004 Harmon adjustable network is used with a model 38 preamp. The IN5 module has six resistors (3 per channel) 26.7K, 8.2K and 5K pot. This module offers a scaling range between 23.5% to 33.1% of the original value. The adjustment range when looking at a 70°C calibrated heat source is 15 mm $\pm$ 2 mm. The .1 μ F capacitors bypass high frequency noise off the input line for each channel. The 1 μ F coupling capacitor AC couples the heat reading to the analog board. The 1.5KE7.5C bidirectional transzorbs shunt transients greater than 7.5 volts to ground.

Interface Module IN4

This module is designated as being for future use.

Interface Module IN3

This module interfaces the ambient temperature sensor to the analog board. This module scales the input down by 7.7% so that it is 92.3% of its original value. The .1 μ F cap is to bypass noise. The 1.5KE7.5C transzorb shunts transients greater than 7.5 volts to ground.

16 Channel Analog Multiplexer

The 16 channel analog multiplexer is made up of IC17 {U26} and IC20 {U27}, which are 8 to 1 multiplexers (MC14051BAL). These are selected one at a time to give 16 to 1 decoding. The multiplexer routes all 16 lines to the A/D converter. These lines include all six pots, heat readings, and DAC generated test signals.

The 8 channel addressing is handled by P60, P61, P62. Chip select is handled by P63 for IC17 {U26} and P64 for IC20 {U27}. The chips are powered by +5 volts and -6 volts to allow for bipolar operation.

16 Channel Analog Multiplexer Control Logic

Address lines P60 - P64 are generated by IC12 {U18} (74HC374 8 bit latch). The address lines that become P60 - P64 are D0out - D4out, which come from IC4 {U13} (74HC244 tri

⁸Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

state buffer). The lines that drive IC4 {U13} are DAT0 - DAT4 which originate on the Universal Processor board.

IC4 {U13} is enabled by IC5 {U16} (74HC32 OR gate) when the control line is low.

Inputs

Heat Input Peak Hold

Note: The channel 1 and channel 2 inputs function identically except for the reference designators and the addresses. Only channel 1 will be discussed; the designators for channel 2 can be obtained from the schematic.

The input is scaled and impedance matched through the IN5 module described above. Each type of IR sensor has a special IN5 network. Without the correct network, the heat readings will be incorrect. **This type of error can only be detected by an incorrect reading on the system when using a calibrated heat source. This problem will not be detected by the self test of the HBD.** When the wheel is between wheel gates the peak hold circuit tracks the peak.

After the input is scaled by the IN5 module the peak hold circuit R94 {R109} 1M Ω resistor and C54 {C49} .022 μ F capacitor tracks to the highest heat input. This reading is passed through IC13B {U28A} (LM224 OP amp) which does not allow a negative heat reading to pass into IC28 {U25} (MC14052BCL dual 4 to 1 multiplexer).

When the wheel leaves the wheel gates IC28 {U25} routes the heat input via CH1PK to the 16 to 1 multiplexer described above. Then IC29 {U29} discharges the peak hold circuit through R105 {R125}. When it is a Servo⁹ Overlay board, R105 {R125} is a 51K Ω resistor; on all other boards, it is a 47 Ω resistor.

Channel Heat Test Signals

Note: The channel 1 and channel 2 inputs function identically except for the reference designators and the addresses. Only channel 1 will be discussed; the designators for channel 2 can be obtained from the schematic.

To provide a method of testing the board, a two channel DAC {two 1 channel DACs on the Analog I} is used to generate heat information and wheel gates. The heat information is generated by the DAC circuit. This information is routed from IC29 {U29} (dual 4 to 1 multiplexer) through R93 {R109} to the input of IC13B {U28A}. IC13B {U28A} will give a 2x gain to this circuit. IC13B {U28A} will not allow a negative signal to pass through.

⁹Servo and ACS are registered trademarks of Servo Corporation of America, Hicksville, New York.

This is passed through IC28 {U25} (dual 4 to 1 multiplexer) which directs this signal back via CH1PK line to 16 to 1 multiplexer. IC28 {U25} is used for both channels 1 & 2, with the X terminals connected to channel 1 and the Y terminals connected to channel 2.

Wheel Gate Test Signals

Note: The channel A and channel B inputs function identically except for the reference designators and the addresses. Only channel A will be discussed; the designators for channel B can be obtained from the schematic.

The HBD generates wheel gate signals from the DAC to simulate wheel gates in the functional test train and functional self test. The wheel gate A signal passes through IC16 {U5} (MC14052BI dual 4 to 1 multiplexer). The test wheel gate is introduced to IC21A {U1A} via the T3GTA {TEST SIG_3} line.

Advance Gate Test Signals

Note: The channel A and channel B inputs function identically except for the reference designators and the addresses. Only channel A will be discussed; the designators for channel B can be obtained from the schematic.

The HBD generates advance signals from the DAC to simulate advance transducer gates in the functional test train, and functional self test. The signal passes through IC16 {U5} (MC14052BI dual 4 to 1 multiplexer). The test advance gate is introduced to IC26B {U2B} via the T5ATA {TEST SIG_5} line.

Power Supply Test Voltages

The Analog board is tested for power supply voltages. These voltages are multiplexed by IC28 {U25} which directs these signals back to 16 to 1 multiplexer. The +5 volts is scaled by R96 {R91} and R97 {R92} to be between 3.25 and 3.65 volts. The -6 volts is scaled by R107 {R94} and R108 {R95} to be between -2.6 and -3.2 volts. The +12 volts is scaled by R98 {R96} and R99 {R100} to be between 2.7 to 3.1 volts. The -12 volts is scaled by R101 {R98} and R102 {R99} to be between -2.7 to -3.2 volts.

Note: Since the DAC circuits are totally different between the two Analog board revisions, they are divided into two different sections.

DAC Analog I {Analog I Board}

The Analog I board has two types of DACs. The first type is an SE5017. This DAC is the one directly attached to the PC board. This DAC is a 8 bit bipolar current output. The digital value is latched into the DAC when the /ENABLE line (/SEL_0_WR for U23 and /SEL_1_WR for U24) are low. The DAC then outputs the correct current for this digital value. OPAMPs U28 C&D serve as current to voltage converters. This DAC generates its own internal reference voltage.

The second DAC type on the Analog I board is an SE5018, with each one mounted on its own daughter board. This DAC is a 8 bit bipolar voltage output device with its own internal voltage reference. The 1M Ω resistor on the daughter board is to provide the offset voltage. When the /LE line (pin 10) goes low, the data is latched into the DAC and it produces the appropriate output voltage. Since this device is a voltage output, U28 C&D are not used and the output is connected into the circuit past the OPAMP feedback resistor.

INSERT ADD IN SCHEMATIC FOR DAC MODIFICATION HERE!

DAC Analog II

The IC14 DAC (AD7226) is a quad 8 bit bipolar voltage output device. Only outputs B (HBD channel 2), and output C (HBD channel 1) are used. These outputs are buffered by IC13 C&D. This OPAMP level shifts the output of the DAC so the DAC operates in a bipolar mode.

The level shifting voltage comes from IC15 REF-02, a +5 volt reference. This reference voltage also provides a reference voltage to the DAC which determines the output voltage from the DAC.

When the /WR line on the DAC goes low the DATA is latched into the DAC and the output is set to new value. The DAC channel selection is controlled by /SEL0 and /SEL1 lines.

Chart Recorder Drive

The DAC output is routed through IC16 (Dual 4 to 1 multiplexer). This routes the DAC signal through IC21 {U1} (LM224 OPAMP C for channel 2) and IC21 {U1} (LM224 OPAMP D for channel 1). The 100K Ω resistor and .01 μ f capacitor on the input to IC21 serve to bypass high frequency noise and dampen the pen drive signal to the chart recorder. IC 21 {U1} increases the gain 1.67 times for proper drive level for the chart recorder. The output transzorbs provide transient protection for the analog board.

DAC Control and Routing

The DAC is programmed by a 8 bit digital signal generated by the Universal Processor board. This data is buffered by IC4 {U13} (74HC244 line receiver) from the internal HBD bus. This buffered data is latched into the DAC when the DAC select lines /SEL0 and /SEL1 are pulled low. The DAC select lines are decoded by IC6 {U15} (74HC138 3 to 8 address decoder).

DAC Generated Signals

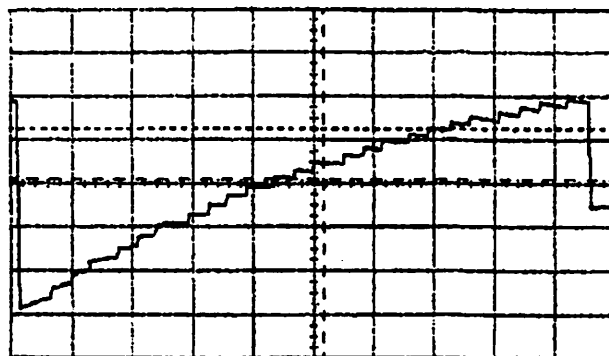


Figure 1: Input to A/D buffer during Self Test.
2V/vertical division, 2ms/horizontal division.

INSERT SOFTWARE EXPLANATIONS OF ALL SIGNALS GENERATED BY DAC.

A/D Converter and Buffer

Note: The Analog I and Analog II boards use different A/D converters so each will be discussed separately.

A/D Converter and Buffer {Analog I}

The analog buffer U22 (LF156 OPAMP) for the A/D converter provides a slight (1.08x) increase in gain. The 200pf capacitor C42 on the input to the OPAMP is to filter out high frequencies.

The Analog I board uses an AD673 A/D converter (U21). This is an 8 bit bipolar successive approximation A/D converter. Each conversion is started with a positive pulse on the convert line (pin 12). While the conversion is in progress /DR (pin 18) is high; when conversion is complete this line goes low. The data is read out when the /SEL_1_RD line goes low (pin 20).

A/D Converter and Buffer Analog II

The analog buffer IC18 (LF156 OPAMP) for the A/D converter provides a slight (1.03x) increase in gain. The 200pf capacitor C30 on the input to the OPAMP is to filter out high frequencies. The two 10K Ω resistors (RP6 A&B) that are on the output and tied to +5VREF bias the input to the A/D converter to 2.5 volts DC, making this a single ended converter. With this bias, (2.5 volts) it is possible to measure bipolar inputs.

The A/D converter is IC19, an ADC0803 8 bit converter. The converter uses an external RC network (RP6 C and C29) to set the internal clock frequency to 620kHz $\pm$ 20kHz. To make a very stable A/D converter the VCC for the converter is the +5VREF voltage, the converter

scales this voltage by half and uses it for its reference voltage. The conversion is started by a low on /WR pin 3, the /INTR will be high while the conversion is in progress. The contents of the A/D converter are read by a low on /RD pin 2.

Digital Output Buffers

The digital output buffers serve to control bus traffic off of the analog board.

The digital output from the A/D converter is buffered to the HBD bus by IC3 {U20} (74HC244 line driver) as signals P10 to P17 into IC3 {U20} and to the HBD bus as DAT0-DAT7. The output from IC3 {U20} is enabled by /SL1RD.

IC1 {U19} (74HC244 line driver) buffers the wheel pickup and advance transducer status bits and the A/D converter status (through conversion) bit. IC1 {U19} is selected by (/BIORD + SEL0).

Digital Input Buffers

The digital input buffers serve to control bus traffic onto the Analog board from the HBD bus.

The input from the HBD bus is buffered by IC4 {U13} (74HC244 line receiver). The output of IC4 {U13} is D0OUT-D7OUT. This chip is enabled by IC5 {U16} (74HC32 OR gate), which determines whether data is entering the Analog board or leaving the board.

The input data is routed to other I/O needs through IC9-IC12 {U9, U10, U11, U18} (74HC374 octal D flip flop).

IC9 {U9} controls the gate A & B positive and negative interrupt enables.

IC10 {U10} controls the advance gates A & B interrupt enables.

IC11 {U11} controls selection of multiplexers IC28 {U25} and IC29 {U29}. These multiplexers control heat input, test heat input, and power supply test voltages.

IC12 {U18} controls selection of the 16 to 1 multiplexers IC17 {U26}, and IC20 {U27}, and the start sample signal of the A/D converter.

Address Decoding

IC5 {U6} (74HC32 OR gate) controls the reading or writing of data to and from the analog board.

IC7, {U14} along with P4, performs the board address decoding based on the P4 jumper setting. This output is active low and is /BIOSEL.

IC6 {U15} (74HC138 3 to 8 decoder) provides addressing to the DAC as /SEL0 and /SEL1. Lines /SEL0 and /SEL1, ORed by IC2 with /BIORD, select line drivers IC1 {U19} and IC3 {U20}, which output data to the HBD bus.

IC6 {U15} also provides outputs /SEL3-/SEL6. These are ORed by IC8 {U12} with /BIOWR to select IC9-IC12 {U9, U10, U11, U18} data input buffers.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections Continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

Analog Board Connector P1

NAME	CONNECTION	TERMINAL BLOCK
CH1 Analog Out	4	TB5-1
CH2 Analog Out	2	TB5-2
CH1 IN5 Input	26	TB7-10
CH2 IN5 Input	25	TB7-9
CH3 IN3 Input	18	TB7-5
CH6 IN3 Input	15	TB7-2
CH4 IN4 Input	17	TB7-4
CH5 IN4 Input	16	TB7-3
Gate Transducer A -	4	TB5-4
Gate Transducer A +	5	TB5-5
Gate Transducer B -	6	TB5-6
Gate Transducer B +	7	TB5-7
Advance Transducer A -	8	TB5-8
Advance Transducer A +	9	TB5-9
Advance Transducer B -	10	TB5-10
Advance Transducer B +	11	TB5-11

The Data Communications Processor 3 (DCP3) is an option card that provides data storage of trains and data communication capability to the HBD.

PART ONE: PHYSICAL DESCRIPTION

The DCP3 board consists of connectors P1, J1 through J5, jumpers W1 through W9, switches S1, S2, and adjustable capacitor C25.

Connector P1

The part of the printed circuit board which slides into the motherboard in the HBD cabinet. P1 has 72 gold-plated pins. P1 supplies power to the DCP3. The DCP3 supplies a power down indicator to the system through P1.

Connector J1

Female DB25 connector mounted on the outside edge of the DCP3. J1 is referred to as either the test terminal or the local port. J1 provides local on site communications via an RS232 port.

Connector J2

20 pin connector mounted on the outside edge of the DCP3. Referred to as the HBWD port, J2 provides communication between the DCP3 board and the time & date board.

Connector J3

20 pin connector mounted on the outside edge of the DCP3. Referred to as the remote port, J3 provides communication via a modem over telephone lines, microwave link, etc.

Connector J4

20 pin connector mounted on the outside edge of the DCP3. Referred to as the AUX port, J4 provides communications to a central office using the optional DCP3 field protocol .

Connector J5

20 pin connector mounted on the outside edge of the DCP3. J5 provides site status information to the DCP3.

Jumper W1

16 position header used to configure communication port 1 (connector J1). Standard DCE settings are : 1-3, 5-7, 9-11, 2-4, 6-8, 10-12, 13-14, 15-16.



Figure 2: W1
DCE Jumper
Configuration

Jumper W2

16 position header used to configure communication port 2 connector J2. Standard DCE settings are : 1-3, 5-7, 9-11, 2-4, 6-8, 10-12, 13-14, 15-16.



Figure 3: W2
DCE Jumper
Configuration

Jumper W3

16 position header used to configure communication port 3 connector J3. Standard DTE settings are : 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16.



Figure 4: W3
DTE Jumper
Configuration

Jumper W4

16 position header used to configure communication port 4 connector J4. Standard DCE settings are : 1-3, 5-7, 9-11, 2-4, 6-8, 10-12, 13-14, 15-16.



Figure 5: W4
DCE Jumper
Configuration

Jumper W5

Enables or disables the battery backup of memory. When disabled, battery life will be increased, but the memory will be lost if power is removed from board.

Jumper W6

Not used.

Jumper W7

Not used.

Jumper W8

Not used.

Jumper W9

Not used.

Switch S1

Four position dip switch. This switch configures the communication parameters of the test port (J1). The specific switch settings are software dependent and will be covered in another section.

Switch S2

Momentary contact push button that causes a reset of the DCP3.

Note: D3 will light momentarily while switch S2 is depressed or system is reset.

C25 Adjustable Capacitor

Used to set crystal oscillator frequency for the real time clock. C25 is factory set and should not be adjusted without explicit instructions from Harmon Electronics.

PART TWO: CIRCUIT DESCRIPTION

The DCP3 card is divided into the following sections:

1. Central Processing Unit (CPU).
2. Address decoding
3. Address Latch
4. Data Bus
5. Bus controller
6. WatchDog timer
7. RAM select
8. RAM
9. ROM
10. Clock Calendar
11. Counter Timer
12. Clock Generator
13. Interrupt Controller
14. Communication port Test (J1)
15. Communication port HBWD (J2)
16. Communication port Remote (J3)
17. Communication port AUX (J4)
18. I/O Address decode
19. Site status input
20. Switch S1 interface
21. LED Control
22. Installed but not Used

CPU Central Processing Unit

IC1 is an Intel 80C88 8 bit microprocessor running at 5 MHz. IC1 has 20 address/data lines and can directly address 1 megabyte of memory.

AD0-AD7 are the address data bus. The bi-directional bus can carry either the lower 8 bits of an address (latched by ALE), or 8 bits of data.

A8-A15 are the upper 8 address lines (latched by ALE). They are used for addressing RAM, ROM, and I/O decoding.

A16-A19 are used for page memory addressing of the 8 RAM chips.

Address Decoding

Address decoding is done by the PLD (IC22), and a 74HC138 3 to 8 multiplexer (IC11).

IC 22 provides selection of ROMs and enables decoding of RAM addresses.

IC 11 decodes RAM chip selection as controlled by A15-A17. Control lines RCS0-RCS7 select RAM chips IC14-IC21 respectively.

Address Latch

IC7 and IC8 are 74HCT373s. They latch address bits A0-A15. IC 22 latches address bits A16-A19.

IC7 latches address bits A8-A15 when the ALE line goes low and holds that address value on the output until ALE goes high.

IC8 latches address bits A0-A7 when the the ALE line goes low and holds that address value on the output until ALE goes high.

IC22 latches address bits A16-A19 when the ALE line goes low and holds that address value on the output until ALE goes high.

The ALE line is generated by the bus controller chip (IC3) and will be discussed below.

Data Bus

IC9 is a 74HC245 noninverting bus transceiver. It provides for bi-directional flow of data on the bus. When the direction line (pin 1) is low, data flows from the data bus to the CPU. When the direction line is high, data flows from the CPU to the data bus. The output enable line must be low for outputs to be active. The direction line and output enable lines are controlled by the bus controller chip (IC3.)

Bus Controller

IC3, an 82C88 bus controller, generates the ALE line, direction line DT-R, data output enable, interrupt acknowledge, memory read, write, I/O read, and I/O write lines.

Signals /S0, /S1, and /S2 from the CPU determine the output activity selected.

The timing clock for IC3 is provided by IC2, an 82C84 clock generator. IC2 also drives the CPU (IC1).

WatchDog Timer

Consists of an LM239 (IC30), the watchdog clock, the PLD watchdog logic (IC47), and Q3, a VN2222L FET.

The watchdog clock consists of an R/C oscillator built around a comparator (IC30). This combination produces a square wave output at 1.4 seconds as determined by the R/C time constant of R7 and C26.

IC47 is the logic control for the watchdog timer. The watchdog clock sets the time required for software to strobe the timer.

The IC47 watchdog logic is selected for reading or writing by the /WTIME signal, which is decoded by IC40, the I/O address decoder. When correctly addressed with the /WTIME line the watchdog timer can have 3 bits of data input or output via DB0-DB2.

A power down reset will also cause the watchdog to reset the system. This signal is generated by IC30. The reference voltage is generated by placing the system 12 volts across a 2.7 volt zener diode. The signal voltage is VCC (5 volts) scaled down to 3.1 volts by resistive divider R23 & R24. When VCC drops below 4.5 volts, the output of IC30 (/PDRST) goes low, causing the watchdog to reset the system.

The watchdog resets the system by having the watchdog logic (IC47) turn on Q3, which in turn pulls the /RST line low. The /RST line signals reset to the clock generator (IC2) which produces a reset pulse with the proper timing to IC1.

RAM Select

RAM chip selection is performed by IC11, a 74HC138 3 to 8 multiplexer. The RAM chips are selected when the output from IC11 goes low. IC11 is enabled by the RAMCS line from IC22 which is part of the address decode circuit.

RAM

The RAM chips, IC14-IC21, are 43256 32K by 8 bit chips. The /CE line from IC11 selects each chip. To read data from the RAM chip the /MEMR line must be pulled low by the bus controller (IC3) and the chip must be selected.

During power up and power down, Q1 (VN2222L) is used to control the RAM read/write line. This line (/RWE) must be low in order to write to memory.

During normal operation, the /RWE line is pulled high by the battery through R1. To request a write operation, IC3 pulls the /MEMW line low. This in turn activates Q1 which pulls the /RWE line low, allowing the write operation to proceed. During a reset or low power condition, however, the /RST line is pulled low. This line is connected to the gate of Q1. The low signal on the gate of Q1 keeps Q1 from activating. This ensures that the /RWE line stays high, disabling writes for the duration of the reset.

ROM

IC12 and IC13 are 27512 64K by 8 bit ROM chips. These contain the core software along with railroad specific software that the CPU uses to operate. Currently only IC12 is used and IC13 is left uninstalled. Selection is via the active low /CE line generated by IC22. The /MEMR line generated by the bus controller chip (IC3) must be low to read from the ROM chip.

Clock Calendar

IC44 is an M6242 battery backed up clock calendar using 4 bit data for input and output.

The crystal oscillator runs at 32.768 kHz. Test Point 1 (TP1) allows access to the internal timing of the clock calendar. The frequency at TP1 should be $65 \pm .2$ Hz.

The clock calendar is selected via /CLKSL from the I/O address decoder (IC40).

The /RST line will place the clock calendar in a standby mode when pulled low. This protects it from getting an accidental write during power up or power down. While in the standby mode clock calendar keeps time, but the write and read functions are disabled.

Counter Timer

IC38, an 82C54, has 3 independent counters and six programmable counter modes.

The counter timer chip select is active low and is generated by IC40, the I/O address decoder, via /ICS0. The /IOR and /IOW lines are used to read and write data when the chip is selected.

The clock driving counters 0 & 1 is generated by the clock generator (IC2) and is approximately 2.56 MHz. The output from counter 1 feeds counter 2. This output is a function of the software values that initialized the counter. The output of counter 2 is IRQ0. This signal is fed to the interrupt controller (IC4).

Clock Generator

IC2 is an 82C84 clock generator driver. The clock generator is driven by a 15.36 MHz oscillator (Y1). The clock output is the crystal frequency divided by 3 (5.12 MHz). The PCLK output is the CLK output divided by 2 (2.56Mhz).

The /RES input is the system reset line generated by the watchdog logic described above. This input will produce an active high reset pulse to the CPU. The clock generator will provide a reset pulse with the proper timing to the CPU.

Interrupt Controller

IC4, an 82C59, can handle up to 8 vectored interrupts, and has programmable priority levels for interrupts.

When IC4 receives an interrupt, it outputs one interrupt via INT to the CPU. The CPU acknowledges the interrupt via IC3 (bus controller). This acknowledgement reaches IC4 on the /INTA line.

The chip is selected by the /INTCS line generated by IC40 for reads or writes.

NOTE: Since the four communication ports are functionally the same, a generic communication port will be presented, with differences between the specific ports following. In the description, an 'x' means a number is different in each port.

Communication Port

Each port consists of an 82C50 UART, a 1488 RS232 line driver, and a 1489 RS232 line receiver.

The UART is a Universal Asynchronous Receiver/Transmitter which produces the baud rate and translates the parallel 8 bits of data to and from the RS232 format. The chip also has capability to control a modem.

The crystal oscillator (Y2) provides a 1.8432 Mhz clock to the UART via the BCLK line.

The parallel data to and from the chip is enabled via /PXCS which is generated by IC40 (IO address decoder).

The interrupt line IRQX goes active high when UART has parallel data (received data) ready.

Sout is the serial data output from the UART to the line driver.

Sin is the serial data input from JX via the line receiver to the UART.

/RTS is the request to send line. It enables the modem when low, indicating that the UART has serial data to send.

/DTR, when low, indicates that the UART is ready to receive serial data.

/DSR, when low, indicates that the modem is ready to exchange data with the UART.

/DCD, when low, indicates that the data carrier has been detected by the modem or data set.

MR is the reset line and when high will force the UART into an idle mode.

RING IN input on JX is level shifted by the 1489 line receiver to logic level and is input on the UART on /RI as a ring indicator.

The 1488 line driver takes logic data from the UART and level shifts it to standard RS232 levels where the output swings to 12 ± 5 volts. The exact voltage level is a function of load.

The 1489 line receiver takes RS232 levels of 20 ± 5 volts and converts it to digital levels for the UART.

The UART provides two general purpose outputs that are software controlled:

- /DTR is level shifted by the 1488 line driver and is SEL1 on JX
- /OUT2 is level shifted by the 1488 line driver and is SEL2 on JX.

Communication Port J1 (TEST Port)

82C50 UART - IC10

1488 RS232 line driver - IC23

1489 RS232 line receiver - IC24

Communication Port J2 (HBWD Port)

82C50 UART - IC25

1488 RS232 line driver - IC27

1489 RS232 line receiver - IC31

Communication Port J3 (Remote Port)

82C50 UART - IC33

1488 RS232 line driver - IC36

1489 RS232 line receiver - IC37

Communication Port J4 (AUX Port)

82C50 UART - IC32

1488 RS232 line driver - IC34

1489 RS232 line receiver - IC35

IO Address Decode

IC40, a 74HC154 4 to 16 multiplexer, decodes the address for the I/O devices, i.e. - J5 site status, watchdog timer, LED array, clock calendar, etc.

Site Status Input

IC45, a 74HCT244, couples the 8 bits of site status information from J5 to the data bus. IC45 is enabled when the chip select line is low.

S1 Switch Interface

IC43, a 74HCT244, interfaces the S1 status to the lower 4 data bits DB0-DB3. The chip is selected by the IO address decoder (IC40), and an OR gate (IC41).

LED Control

IC42, a 74HCT374, controls the 4 LEDs on the outside edge of PC board when instructed to do so by the software. The LEDs are controlled by the lower 4 data bits DB0-DB3. The chip is selected by the IO address decoder (IC40), and an OR gate (IC41).

Not Used but Installed

The following circuits are on the board but are not used at this time.

IC30 and R12-R16 detect a low battery and drive line /BTLOW.

IC46 PLD is not used at this time.

PART THREE: SIGNAL DESCRIPTIONS

/MEMW Memory write cycle - indicates data write cycle.

/MEMR Interrupt request from counter timer IC38 82C54.

IRQ1 Interrupt request from UART IC25 82C50, HBWD comm.

IRQ2 Interrupt request from UART IC32 82C50, AUX comm.

IRQ3 Interrupt request from UART IC33 82C50, REMOTE comm.

IRQ4 Interrupt request from UART IC10 82C50, TEST comm.

IRQ5 Not used.

IRQ6 Not used.

IRQ7 Not used.

PCLK	Clock signal to IC38 counter timer 82C54.
CLK88	Clock signal to IC1 processor 8031, and IC3 bus controller 82C88.
/PCS0	ROM select IC12.
/PCS1	ROM select IC13.
/RCS0	RAM select IC14.
/RCS1	RAM select IC15.
/RCS2	RAM select IC16.
/RCS3	RAM select IC17.
/RCS4	RAM select IC18.
/RCS5	RAM select IC19.
/RCS6	RAM select IC20.
/RCS7	RAM select IC21.
RAMCS	RAM address decode enable.
/RWE	RAM write enable.
ALE	Address latch control.
/RST	Reset line from watchdog to IC2 clock generator.
PRST	Reset line to IC1 processor 8031, from IC2 clock generator 82C84.
VBAT	Battery voltage from battery backup.
/PDRST	Power down reset to watchdog timer.
WDCLK	Clock for watchdog timer.
WDRST	Watchdog timer reset line.
ICS0	Chip select for IC38 counter timer 82C54.
/INTCS	Chip select for IC4 interrupt controller 82C59.

/P1CS	Chip select for IC10 UART 82C50.
/P2CS	Chip select for IC32 UART 82C50.
/P3CS	Chip select for IC25 UART 82C50.
/P4CS	Chip select for IC33 UART 82C50.
/CLKSL	Chip select for IC44 clock calendar.
/ICS1	Chip select for IC42 LED driver.
/ICS2	Chip select for IC45 Site Status.
/WTIME	Chip select for watchdog timer logic.

HBD Internal Bus Connections

NAME	CONNECTION	DIRECTION
DAT0	9	I/O
DAT1	K	I/O
DAT2	10	I/O
DAT3	L	I/O
DAT4	11	I/O
DAT5	M	I/O
DAT6	12	I/O
DAT7	N	I/O
ADR0	8	O
ADR1	J	O
ADR2	7	O
ADR3	H	O
ADR4	6	O
ADR5	F	O
ADR6	5	O
ADR7	E	O
ADR8	20	O
ADR9	X	O
ADR10	19	O
ADR11	W	O
ADR12	18	O
ADR13	V	O
ADR14	17	O
ADR15	U	O
ADR16	26	O
ADR17	d	O
ADR18	27	O
ADR19	e	O
/PSEN	28	O
CLOCK	29	O

HBD Internal Bus Connections continued

NAME	CONNECTION	DIRECTION
/RESET	h	O
/RD	22	O
/WR	z	O
/DIR	23	O
/MEM-RQ	24	O
/I.O.RQ	b	O
/MEM-EX	25	O
/PWR DWN	30	I
MPRO	j	O
+12V	33,m	PWR IN
+5V	3,4,C,D	PWR IN
GND	1,8,M31,32,A,B,k,C	GND
COM	36,r	COM
-12V	34,n	PWR IN

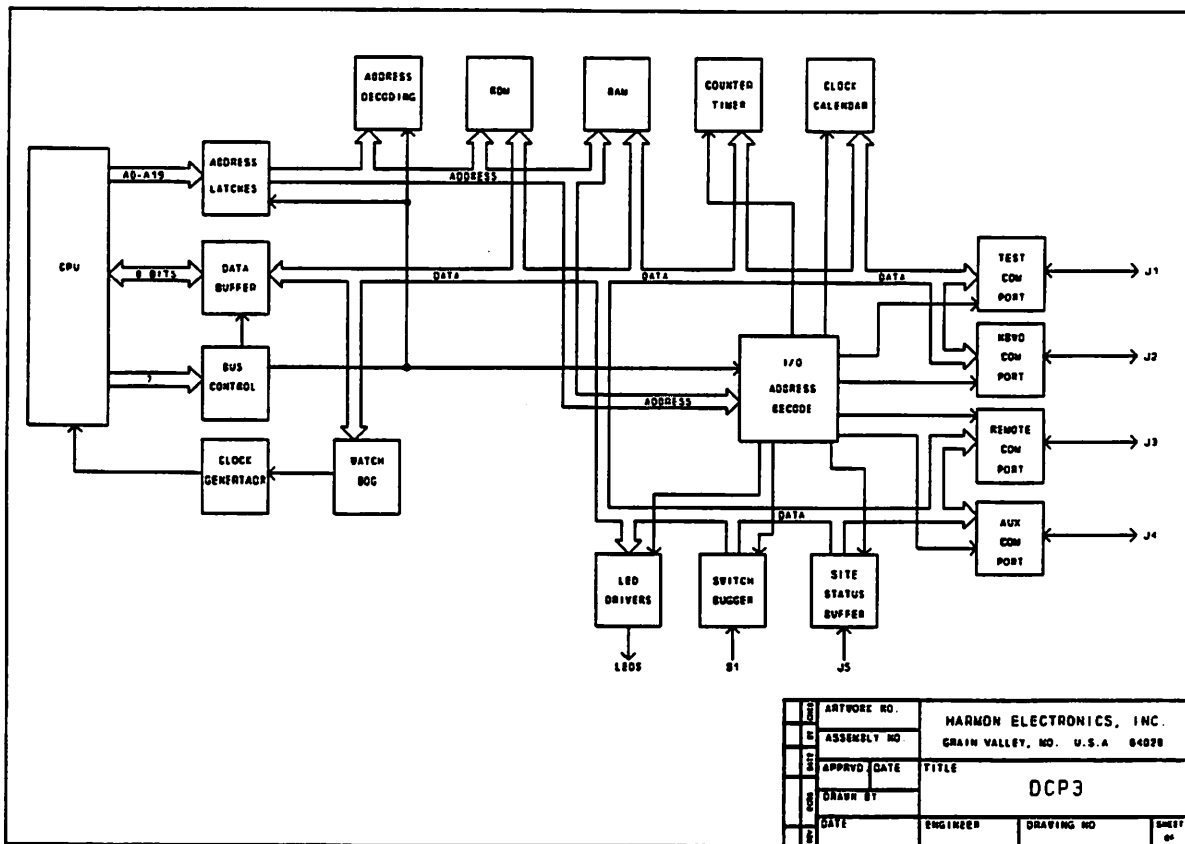


Figure 6:
DCP3 Block Diagram

The power supply supplies 47 VDC preamp power, 39 VDC reference shutter supply. The power supply also has a 24 VDC unfiltered power supply.

PART ONE: PHYSICAL DESCRIPTION

The power supply mounts in a 19" rack. The unit is all hand wired. The power supply consists of two transformers T1, T2 a terminal blocks TB1, and TB2.

Transformer T1 converts 120 VAC to 63 VAC for the 47 VDC supply.

Transformer T2 converts 120 VAC to 31 VAC for the 24 VDC supply.

Terminal block TB1 outputs the DC power supply voltages for 47, 39, and 24 VDC.

Terminal block TB2 is the AC voltage connection for snow heaters.

PART TWO: CIRCUIT DESCRIPTION

The power supply can be divided into the following sections:

1. AC voltage input
2. Transformer T1
3. Transformer T2
4. 47 VDC regulator
5. 39 VDC supply
6. 24 VDC supply

AC voltage input The power supply is powered by 120 VAC. The 120 VAC is current limited through power resistors R101 and R102. The input filter capacitors C101 and C102 filter an high frequency noise on input. The surge protector SP1 will short high voltage transients on the input 120 VAC line to ground.

Transformer T1 takes the input and steps it down to an isolated 63 VAC for the 47 and 39 volt power supplies. The output of the transformer passes through circuit breaker CB2. The AC voltage is rectified by full wave bridge rectifier CR1.

Transformer T2 takes the input and steps it down to an isolated 31 VAC. The output of the transformer passes through circuit beaker CB3. The Ac voltage is rectified by full wave bridge rectifier CR2.

47 VDC Regulator C103 provides AC noise filtering of the regulator. The transistor Q1 is always forward biased and provides a current control for the 47 volt regulator. U1 LM217K is the regulator, R7 & R8 are part of the voltage feed back for the regulator. The variable

resistor R9 allows adjustment of the 47 volt supply from 41 to 52 volts. The capacitors C5 and C4 provide output filtering for the 47 volt power supply. The zener diode CR6 is to prevent excessive voltage on the output of the 47 volt power supply. If the voltage is in excess of 56 V the diode will begin to conduct.

39 VDC Power Supply The reference shutter 39 volts is supplied CR2, and CR3 volt zener diodes. The current from the 47 volt supply flows through R6 and CR3 (39V drop across CR3) to produce the 39 volts output on TB1-12. The current from the 47 volt supply flows through R3 and CR2 (39 V drop across CR2) to product the 39 volts output on TB1-11.

24 VDC Power Supply The 24 volts is unregulated, C1 provides a high frequency by pass and RV1 MOV provides transient protection for the output.

The ambient temperature sensor provides a linear output voltage proportional to the temperature. The ambient temperature sensor is powered by +12 volts from the hot box detector.

PART ONE: PHYSICAL DESCRIPTION**Pot R6**

Factory adjusted to calibrate the sensor's output voltage. This should not be adjusted in the field.

Cable

Three conductor cable that interfaces the sensor to the Hot Box Detector. The cable supplies +12 volts and ground to sensor. The cable carries the output voltage from the sensor to the Hot Box Detector.

PART TWO: CIRCUIT DESCRIPTION

The ambient temperature sensor converts temperature to voltage for a slowly changing temperature. The formula for this is as follows:

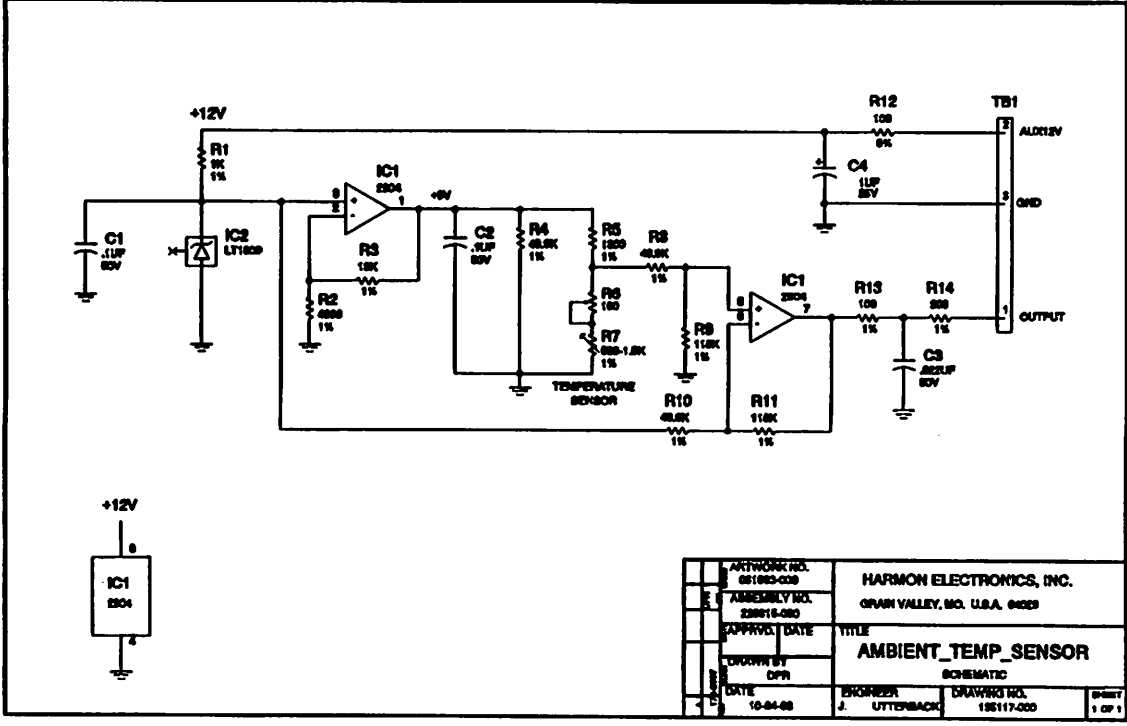
$$V_{out} = (55 + TA) * .040$$

where TA is the ambient temperature. The two constants determine the offset and the slope of the output function. 55 is the offset, which means at -55 °C the output from the sensor is 0 volts. The output voltage changes 40 mv for every degree change. When at 20 °C the output will be $(55 + 20) * .040$ or 3.0 volts.

The circuit is powered from the HBD 12 volts, R12 is in series with the power source to prevent system failure due to a power short in a sub assembly. This 12 volts is used to power IC1 and provide a source voltage for IC2. IC2 is a 2.5 volt reference that is designed to provide a stable reference over temperature. This 2.5 volt reference is used by the circuit for two functions. The first function is to provide a stable voltage source voltage to the temperature sensor regardless of source supply variances. The source voltage of 9 volts to the temperature network is provided via IC1A which provides a positive voltage gain of 3.6 and produces an output of 9 volts at 20 ma. The second function of the 2.5 volt reference is to provide an offset voltage for the difference amplifier.

The temperature sensing network is comprised of R4, R5, R6, and R7 is the actual temperature sensing device and will change resistance in a linear response to temperature. R5 sets the slope (.040 from equation), and R6 adjusts the offset (55 from equation). R4 is provided as a further linearization method to factor out any small error in a part.

This network produces a voltage that is proportional to temperature and ranges from 2.5 volts to 4.87 volts. This voltage is then input into the difference amplifier with a 2.5 volt reference on the negative input. This 2.5 volts is subtracted from the positive input and the results multiplied by 2.36 resulting in the required output levels. At -55 °C the output from the resistor network would be 2.5 volts from this and multiply by 2.36 so the output should be $(2.5 - 2.5) * 2.36 = 0$ volts. This value would then match the mathematical model of VOUT. This voltage is output via R13, R14 and C3 to provide a lowpass filter and an output impedance of 300Ω.



Data Communications Processor II

The DCP II Accessory Board is a STD Bus size card for the DCP II system. It provides additional features such as LED indicators, push button reset switch, reset LED indicator, User jumper selections and additional RS-232 line support.

PART ONE: PHYSICAL DESCRIPTION

The DCP II accessory Board contains bus connector P1, connectors J1, J2 and J3, 3 board select jumpers, 6 user selectable jumpers, 4 LED indicators, a push button reset switch, a Reset LED Indicator, 8 bits of digital input, 2 RS-232 line drivers and 2 RS-232 line receivers.

Connector P1

The part of the printed circuit board that is inserted into the DCP II chassis motherboard.

Connector J1

J1 consists of a 16 pin header style connector. J1 connects the 8 digital input bits to the Terminal Block on the rear panel of the DCP II chassis.

Connector J2

J2 is a 14 pin header style connector. J2 is connected to the SI/O board in the DCP II system for serial communications.

Connector J3

J3 is a D style 25 pin connector. J3 is the Local port that is connected to the external modem.

Board Select Jumpers

Used to select a specific address for the DCP II Accessory Board. The board is normally configured with jumper JA5 at position 2-3, jumper JA6 at position 2-3 and jumper JA7 at position 2-3.

User Selectable Jumpers

Labeled as JD2 - JD7 and used for on site configurations of software. They can be set in two possible settings: a jumper across position 1-2 or a jumper across position 2-3.

LED Indicators

Used to display the status of software diagnostics and during power-up to show that a particular test is being performed.

Push Button Reset

Allows the DCP II processor board to be reset. Since this signal is connected through the DCP II bus, all other devices are reset also.

Reset LED Indicator

Shows that the Push Button Reset is currently being pressed or that the system is currently in a hardware reset.

8 Bit Digital Input

Connected to a terminal block on the back panel of the DCP II chassis to allow user inputs of digital levels or to connect jumpers across the terminal blocks to select user configurations.

RS-232 Line Driver

Used to transmit two additional signals to the RS-232 interface connected to the Local port of the DCP II system.

RS-232 Line Receiver

Used to receive two additional signals from the RS-232 interface connected to the Local port of the DCP II system.

PART TWO: CIRCUIT DESCRIPTION

The DCP II Accessory Board is divided into the following sections:

1. Address decoding circuit
2. Input/Output port select circuit
3. 8 Bit Digital input buffer
4. User Jumper selections and RS-232 input buffer
5. LED Indicators and RS-232 output buffer
6. Reset Switch and Reset LED Indicator circuit

Address Decoding Circuit

IC2, a 54HCT85 4 bit comparator, compares two sets of 4 bit inputs to generate an active high output of A=B. IC2 compares address lines A5, A6 and A7 to the board address selectors JA5, JA6 and JA7 along with comparing the /IORQ signal from the DCP II bus to a logical low signal in order to generate an A=B output signal. This signal is used to enable IC1 and is also inverted through a NOR gate of IC9 to generate an active low signal to enable IC6.

Input/Output Port Select Circuit

Consists of IC1 which is a 3 line to 8 line demultiplexer. IC1 decodes address lines A0 - A1 and is enabled by an active high signal generated by IC2s A=B output. The decoded outputs of IC1 are /SEL0, /SEL1 and /SEL2.

8 Bit Digital Input Buffer

Consists of IC3 which buffers the eight external connections to the DCP II bus and is enabled by the signal /SEL0. IC3s inputs are pulled up to +5 volts by resistor pack 1 and are current limited for input protection by resistor pack 2.

User Jumper Selections and RS-232 Input Buffer

Consists of IC5 and IC4. IC5 buffers the RS-232 line receivers and the User jumper selections to the DCP II bus and is enabled by the signal /SEL1. Pins 2 and 4 of IC5 inputs signals from IC4 which is an RS-232 line receiver. IC4 converts the RS-232 standard level inputs to a digital level for use in adding the signals of Data Carrier Detect and Ring Indicate from the Local port to the DCP II system. Pins 6, 8, 17, 15, 13 and 11 are connected to JD2 - JD7 respectively. These jumpers can be configured for two possible settings: a jumper across position 1-2 will pull the inputs low, or a jumper across position 2-3 will allow them to be pulled high by resistor pack 3.

LED Indicators and RS-232 Output Buffer

Consists of IC7 and IC8. IC7 buffers data from the DCP II system bus to the 4 LED Indicator lights and to the RS-232 line drivers. IC7 is enabled by an active high signal that is generated by a NOR gate of IC9 which combines the signals /WR from the DCP II system bus and /SEL2 output from IC1. Outputs Q0 - Q1 are connected to IC8, which is an RS-232 line driver chip used to convert the digital levels of these two lines to the signal levels that comply with the RS-232 standards. Outputs Q2 - Q5 of IC7 are used to drive the four LED Indicator lights and use resistor pack 4 for current limiting. Outputs Q6 - Q7 are not currently used.

Reset Switch and Reset LED Indicator Circuit

Consists of IC9, an LED indicator, a push button momentary contact switch and two resistors. The signal PBRST that is connected to the DCP II bus is normally pulled high through a resistor in resistor pack 3. PBRST is pulled low when S1 has been pressed to reset the system. The signal SYSRST is connected from the DCP II bus to a NOR gate of IC9 that logically inverts the signal. This signal is inverted again by another NOR gate of IC9 to drive the cathode side of the Reset LED. A resistor of resistor pack 4 is used for limiting the current to the LED.

PART THREE: SIGNAL DESCRIPTION

- | | |
|--------------|--|
| /WR | This signal is generated on the DCP II Processor Board and is interfaced to this board via P1. /WR is used to control Write operations to the on board output ports. |
| /RD | This signal is generated on the DCP II Processor Board and is interfaced to this board via P1. /RD is used to control Read operations from the on board input ports. |
| /IORQ | This signal is generated on the DCP II Processor Board and is interfaced to this board via P1. /IORQ is used in conjunction with /WR and /RD for on board Input/Output operations. |
| /SEL0 | This signal is generated on board and is used to enable the input data buffer IC3 for the 8 digital input lines. |

- /SEL1** This signal is generated on board and is used to enable the input data buffer IC5 for the User Jumper selections and the RS-232 line receivers.
- /SEL2** This signal is generated on board and is used in conjunction with the /WR signal through a NOR gate of IC9 to enable the output data buffer IC7 for latching data to the 4 LED Indicators and to the RS-232 line drivers.
- SYSRST** This signal is generated on the DCP II Processor Board and is interfaced to this board via P1. SYSRST is used to display that the system is in a reset state by illuminating the Reset LED Indicator.
- PBRST** This signal is generated on board and is used to generate a hardware reset condition for the entire DCP II system when switch S1 is closed momentarily.

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Data Recall

Main Boards Used

UNIVERSAL PROCESSOR BOARD

Theory of Operation

The Hot Box Detector contains a circular buffer (recall buffer) that is capable of storing data for four (4) trains. The information saved for each train is in a summary format, the axle heat values are not saved. The criteria for saving trains in the recall buffer are :

- ◆ Train must be a real train. Test trains are not stored in the recall buffer.
- ◆ Train must have at least one defect. Defects can be either Hot Journals or AUX alarms.

It is important to note that integrity failures and/or warnings are not part of the criteria for storage. For example, if a train has an integrity failures and/or warnings, but no defects, it is not be saved in the recall buffer.

The function of **DATA RECALL** is to simulate the same environment as the End Of Train state for a particular train. Therefore the End Of Train service routines process the data as if a real train has just passed the detector. The same EOT operations are performed for the simulated environment (same EOT messages, and chart recorder data).

DATA RECALL can be divided into four major parts, as follows:

- ◆ Storing train data.
- ◆ Pre-function initialization.
- ◆ Simulation of End Of Train environment.
- ◆ Post-function initialization.

Each topic will be described in more detail in the following sections. Before the actual discussion of the **DATA RECALL** function, the following must be noted:

1 - The RAM space on the CPU board provides the memory for the recall buffer. The contents of RAM are lost during any power loss. Therefore, the contents of the recall buffer will be lost if any power loss occurs.

2 - The first step in **DATA RECALL** is to calculate the checksum for the stored data. If the calculated checksum does not equal the checksum stored as part of the data, the data for the particular train will be deleted. As with other HBD operations, the software protect itself from bad memory (or memory circuits) by using the checksum technique. In this case, a proper message will be displayed, informing the user of the memory failure.

Recall Buffer

The recall buffer consists of four segments, each large enough to hold summary data for one train. Each segment is 128 bytes long. The First In First Out (FIFO) procedure is employed to manage the recall buffer. Therefore, the most recent train over-writes the oldest train. Figure 1 demonstrate the FIFO operation.

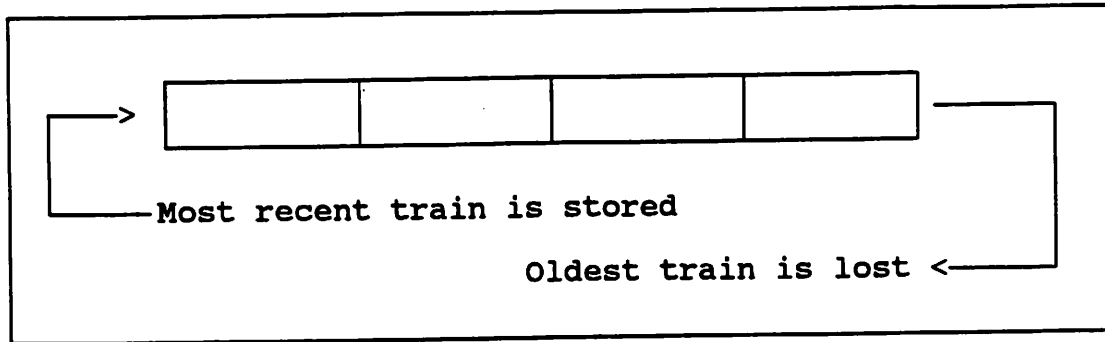


Figure 1. First In First Out

Internally the HBD manages the buffer by using a pointer, addressing the next available segment. This pointer either addresses an empty segment, or points to the oldest train data. Using the pointer, train data does not need to be moved around in the recall buffer. Figure 2 and 3 demonstrate the use of pointer.

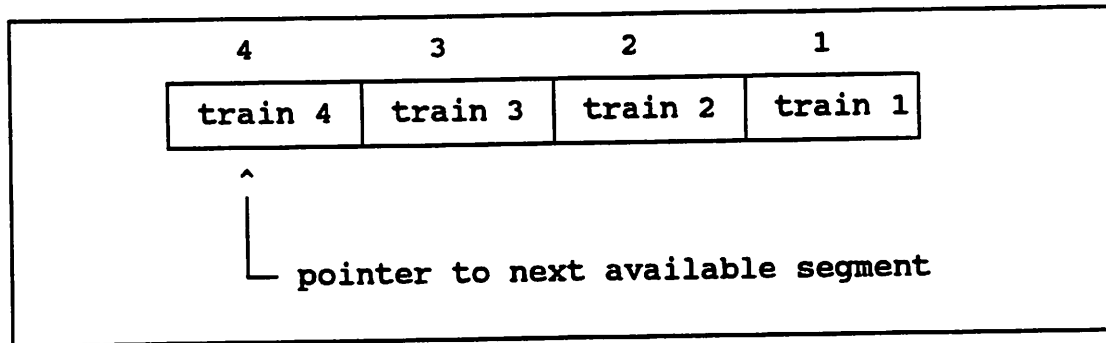


Figure 2.

On system power up the pointer points to the first segment of the recall buffer. After storing the first train, the pointer is incremented, so that it points to the second segment. Once the pointer points to the fourth segment, it is reset to point to the first segment. As shown the work load is at its minimum using the pointer technique, which requires only one addition, versus moving the data for three trains (384 bytes).

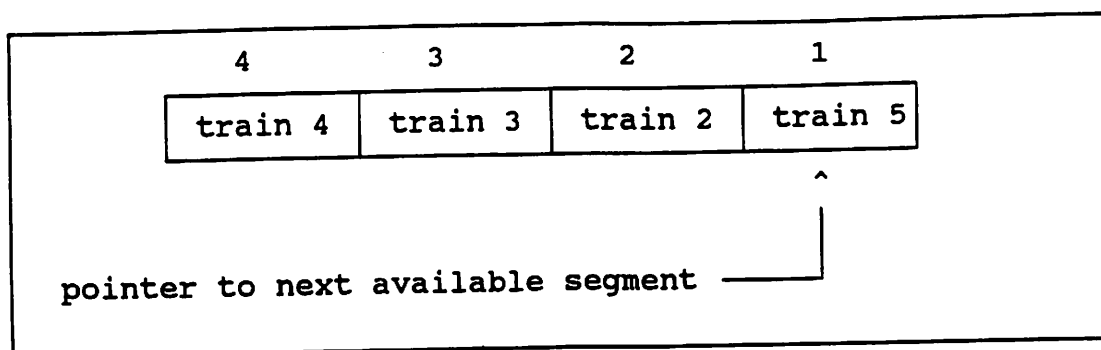


Figure 3.

As mentioned previously, each segment of recall buffer consists of 128 bytes. Figure 4 shows the structure of each segment. The first 80 bytes which are used for alarm data can store up to 16 alarms per train. The next two bytes are the checksum for the alarm data. The checksum bytes are used to determine the integrity of stored data at a later retrieval. The third field of each segment (46 bytes) contains the integrity data and train data. Finally the last two bytes of each segment contain the checksum for integrity and train data.

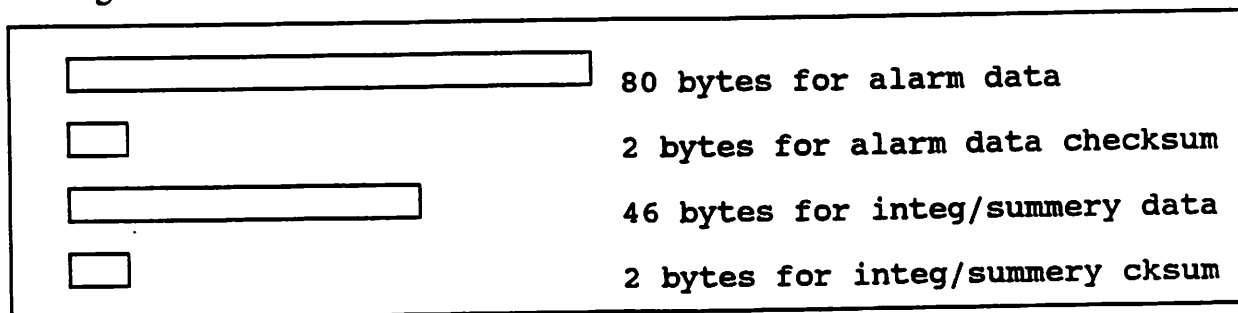


Figure 4. Data Recall Memory Allocation

The first 80 bytes of each segment can store up to 16 alarms. 5 bytes are assigned to each alarm. These are :

- ◆ Heat Alarms : Bit encoded, signifies possible heat alarms for the axle.
- ◆ AUX Alarms : Bit encoded, signifies possible auxiliary alarms for the axle.
- ◆ Axle Status : Bit encoded, signifies axle data (first axle of car, out of sync axle, etc.). and type of heat alarm (absolute, differential, etc.).
- ◆ Axle Number : Axle number.

The 46 byte field stores detector status and train summery data. 20 bytes are used to store the detector status (integrity failures/warnings) for the last train to cross the detector. Most of these bytes are bit encoded, signifying up to 60 possible integrity failures/warnings. The remaining bytes are used to store train data such as; train speed, number of axles, number of cars, inside/outside temperature, time and date of train passage, etc.

End of Train Service Routine

This section describes some of the operations (related to data recall) which are performed by the End Of Train service routine. The EOT service routine is activated when the timeout timer has expired. The timeout timer (10 seconds) is reset every time an axle crosses the leading wheel gate transducer. Thus the HBD enters its EOT stage 10 seconds after the last axle has crossed the leading gate transducer.

The following operations are performed by the EOT service routine:

- ◆ The End Of Train message is transmitted to the train crew.
- ◆ The End-Of-Train data is routed to the chart recorder.
- ◆ If the current train is a real train, and the train has at least one alarm, its data is stored in the recall buffer.
- ◆ System variables are re-initialize for the arrival of the next train.

Data recall simply constructs an environment similar to the End-Of-Train stage of a particular train. The environment is constructed by loading the system variables with the processed data. At this point the EOT service routine is called. The EOT service routine uses the data which has been processed by the Train Passing service routines. In other words, the EOT service routine is not aware of the fact that its data has been loaded by the data recall routine. Thus the same procedure which applied to the real train passing the detector, is also applied to the stored data. There are, however, a few differences between a real train EOT data processing, and the recall data processing. These differences are described in the following sections.

Storing Train Data

As described previously, if a real train passes the detector, and has at least one alarm, its data will be stored in the recall buffer. To do so, the segment designated by the recall buffer pointer is used to store the data. Therefore the train data stored in this segment is over-written by the current train data. The pointer is also incremented to point to next available segment. The checksum fields are computed and stored as part of the train data.

This step (storing train data) is by-passed, if EOT service routine has been activated by the Data Recall routine. Therefore a recalled train can not over-write another train.

Data Recall Execution

The Data Recall routine is activated when the MODE is placed in the DATA RECALL.

The DATA RECALL routine prompts the user by displaying "RECALL?" phrase at the DATA DISPLAY, and monitors the front panel DATA ADV switch. To start the recall procedure, the user must press the DATA ADV.

Upon activation of the **DATA ADV** switch, the recall routine performs the following:

- ◆ "RECALL 1" is displayed. The number displayed represents the most recent train in the recall buffer. Therefore, '1' signifies the most recent train, while '2' signifies the second most recent train, and '4' signifies the oldest train in the buffer. At this point, the recall routine delays its execution for two seconds. The user can press the **DATA ADV** switch during the two second wait period. Every time the **DATA ADV** switch is activated, the digit which signifies the train index is incremented. The **DATA DISPLAY** is updated, informing the user of his/her selection. The user can select any of the available trains in the recall buffer, by pressing the **DATA ADV** switch within the two second wait period (the two second timer is reset to zero upon pressing the **DATA ADV** switch).
- ◆ Once the two second wait period has expired, the recall buffer status is examined for presence of the selected train. If the desired train does not exist (segment is empty), the phrase "NO DATA" will be displayed. At this point the recall routine ends its execution by re-displaying "RECALL?".
- ◆ Next step is to compute the checksum for stored data, and compare it against the stored check sum. In case of a bad check sum, the phrase "BAD DATA" will be displayed, informing the user of the memory failure. Once again the recall routine ends its execution by re-displaying "RECALL?".

However, if the checksum test is successful, the recall routine will save the current status of system variables.

Pre-function Initialization

The pre-function initialization is activated before the execution of train Data Recall. At this point, the current environment must be saved, so that it can be restored after a particular train has been recalled.

The HBD performs its system integrity test once every two minutes. Other environment data are collected once every 50 milliseconds, i.e. temperature, pot settings, etc. Therefore the HBD can restore its environment data in a maximum of two minutes. However, the pre-function initialization is performed as a precaution. The environment data must be restored, if a train arrives within the next two minutes.

Simulation of End of Train Environment

This step simulates the operations performed by the Train Passing service routines. This is accomplished by loading the system variables with the stored data. The 124 bytes of information stored for each train can simulate the exact environment similar to the time train was passing the detector.

The EOT environment is restored by loading the alarm buffer, and train variables such as train speed, number of axles, number of cars, inside/outside temperature, etc.

Once the system variables have been loaded, the End Of Train service routine is activated. Although the EOT routine can identify its caller (real train passing, or Data Recall), it will perform the same operations on the available data. The identity of the caller, however, is used during the following operations:

- ◆ Storing train data. This operation is by-passed if the caller is Data Recall.
- ◆ Triggering the radio. This operation is by-passed if the caller is Data Recall.
- ◆ Re-initialize system variables. If the caller is the Train Passing routine (real train), all the system variables are reset for the next train. However, if the caller is the Data Recall, post-function initialization is performed.

Post-function Initialization

The post-function initialization restores the detector status to pre-data recall status. All the system variables (board integrity status, temperature, etc.) which were saved during step 1 are restored to their previous values.

HBD Test Trains

Main Boards Used

ALL HBD BOARDS

Theory of Operation

The Harmon Electronics, Inc. Hot Box Detector (HBD) offers two types of test (simulated) trains to examine operation of the HBD system. Although the HBD has the capability to test its boards individually the test trains examine the operation of all boards and trackside equipment in real time operation as a complete unit. The simulated test trains can be used to test the following:

- * Test operation of HBD as a unit.
- * Test vocabulary (format/phrases) of HBD messages.
- * Test integrity of HBD boards.
- * Scanner integrity test.
- * Communication between HBD and DCP.

The HBD software generates signals through the universal processor board and the analog board that simulate the passage of a train. Train simulation is divided into two parts; the first unit generates the signals necessary for simulation, and the second unit processes the signals (data) as if a real train was passing.

Note: The processing unit is same as the one which processes a real train. The two units of the HBD work independent of each other making test trains a valid and important tool in exercising the operation of the HBD.

The remainder of this section is devoted to test trains.

1. How to implement a test train.
2. The results of a test train.
3. How the software simulates a test train and the circuitry involved.

HBD Front Panel Display and LEDs

When the **MODE** switch is set to the **FUNCTIONAL SELF TEST** for a functional self test train or position "E" for a continuous test trains the **DATA DISPLAY** shows the "STANDBY" phrase and the clock LED flashes on and off, indicating that the HBD is active. If the **DATA DISPLAY** shows "INTEGRITY", the HBD is performing a two minute integrity test. A test train cannot be initiated while the HBD is performing an integrity. After a test train has been started the **DATA DISPLAY** changes to "APPROACH", indicating train arrival. After a short delay (depending on speed of simulated train) **DATA DISPLAY** will show the speed of the simulated train.

The "WHL GATE" LED will start flashing. The wheel gate LED is on when the HBD simulates an axle (processing unit receives an axle arrival interrupt) and goes off at the end of the simulated axle (processing unit receives axle departure interrupt). The remaining 6 LEDs illuminate when the HBD detects an alarm. Each LED represents a specific alarm as labeled to their right side.

Test Trains Versus Real Trains

The HBD processing unit processes a simulated train as if a real train is passing the detector. During simulated train passage if an alarm occurs the HBD uses the same vocabulary format to annunciate the alarm(s). The End-of-Train message and data sent to the chart recorder is also in the same format as a real train.

There are two exceptions in processing a test train as compared to a real train. First the radio is not keyed on for a test train, and the HBD speech messages can only be heard via the local speaker. Second the HBD does not store test train, regardless of the number of alarms/integrity failures, in **DATA RECALL** memory. Test trains are however transmitted and stored in the DCP. DCP commands can be used to study the test train in more details.

Functional Test Trains Versus Continuous Test Trains

The HBD is capable of generating two types of test trains; functional self test (position **FUNCTIONAL SELF TEST**), and continuous test train (position "E"). The functional self test train has a pre-defined number of axles, cars, heat values, and auxiliary alarms. The number of axles generated is always the same for these type of trains - 172 axles. The number of cars should also be the same, if the train speed has not been changed during the simulated train passage - 42 cars. The outcome of car recognition might be different than documented if the train speed is varied by changing the position of the **FUNCTION** switch during train passage. Heat values for the simulated train should be close to those documented. Minor differences might be seen between slow train, and fast trains and between different analog boards. This is due to the fact that the simulation unit uses different delays to generate axles and heat value signals and analog board components tolerances are not exactly the same.

Although the functional self test train has been programmed with a specific number of alarms the actual number of alarms might be different as documented. Heat alarms depend on the current setting of the alarm levels. By changing the Low limit for example, the number of alarms simulated can be changed. Since the processing unit reads the actual digital port 0 for auxiliary alarms, more auxiliary alarms can be introduced by grounding the alarm inputs.

The continuous test train only generates generic 4 axle cars - up to 999 axles. It does not input heat signals, or auxiliary alarms. Alarms can be introduced at any time as needed, by grounding the specific **AUX** alarm input or placing a heat source in front of the scanners.

The processing unit of HBD works the same for both types of trains. Simulation although is different for the two trains. In the following sections the difference between the two simulated

trains are explained. Most of the simulation logic, however, remains the same for the two trains.

DCP Test Train Commands

The DCP offers the 'T' command in the **DISPLAY MODE** to generate the test trains. The simulated trains are all functional self test trains. 'T1' is used for slow trains, 'T2' is used for medium trains, and 'T3' is used for fast trains. The HBD however, will reject the test train command from the DCP if any of the following situations exist:

- * If the HBD is processing a real train.
- * If the HBD is generating a test train.
- * If the **CHOP** mode is in use.
- * If "Recorder Calibration" is being performed.
- * If the HBD is performing a two minute integrity test.
- * If the HBD has been disabled.

The commands mentioned above are used to generate the functional self test trains. The DCP does not initiate a continuous test trains. Note: The speed of the train is the only variable in the commands. All test trains generated via the DCP will have the same direction.

HBD Front Panel Switches:

If the **MODE** switch is set to the "**FUNCTIONAL SELF TEST**" position the HBD **DATA DISPLAY** shows "**STANDBY**". The exception to this is when the HBD is performing a 2 minute integrity test, then the **DATA DISPLAY** will show the phrase "**INTGRITY**". The two minute integrity test takes about 5 seconds to perform its task. During this period a test train cannot be generated.

The following are the functions of the front panel switches to generate and control test trains.

The **FUNCTION** switch is used to set/adjust the relative speed of the simulated train. The following table shows the three possible train speeds:

Position 1 (left side)	slow train	32 MPH.
Position (middle)	medium train	64 MPH.
Position 2 (right side)	fast train	132 MPH.

Note: The speed of a train can be varied during train passage. The function switch is monitored during the period of generating signals for test train. If it has been changed the HBD takes proper steps to adjust the speed of test train. Also if the position of the **FUNCTION** switch is changed during the test train passage, the car recognition might fail on several axles. This is due to the fact that the first few axles in a car might have different speeds (different axle spacings) than the last few axles.

The **DATA ADV** switch is used to start the test train, and to determine the direction of the test train. To start a functional test train place the **MODE** switch in the "FUNCTIONAL SELF TEST" position and press the **DATA ADV** switch. For a continuous test train, the **MODE** switch must be in position "E" while pressing the **DATA ADV** switch. The HBD takes over from this point on and generate the signals necessary to simulate a train.

The test trains have the same direction regardless of which way the **DATA ADV** switch was pressed. Refer to HBD front panel DIP switch settings for train direction. Once the **DATA ADV** switch has been pressed, the HBD waits 2 seconds while it monitors the **DATA ADV** switch. Direction of the simulated train can be changed during the 2 second wait period by pressing the **DATA ADV** switch again. During the 2 second wait period, the HBD reverses the train direction every time the **DATA ADV** switch is pressed. For example, if the HBD generates North bound test trains as default pressing the **DATA ADV** switch twice simulates a South bound train.

The **RESET** switch cancels a test train. If the **RESET** switch is pressed the HBD stops the simulation unit and resets all its variables to the no train around state. Note: Arrival of a real train (signal from advance transducer, track circuit, or gate transducers) stops the test train automatically.

The steps mentioned above applies to both functional and continuous test trains. The front panel switches play the same roll regardless of train type. The only difference is the position of **MODE** switch. If the **MODE** switch is set to the "FUNCTIONAL SELF TEST" position a predefined test train is generated. If the **MODE** switch is set to position "E", however, a continuous test train (maximum of 999 axles, no heat or aux alarms) is generated.

Ending Test Train Simulation

The functional self test trains have a pre-defined number of axles. Once simulation has been started the HBD ends the simulation after generating 172 axles.

For continuous test trains, however, the **DATA ADV** switch must be pressed to stop the simulation process. The simulation unit for continuous test trains monitors the **DATA ADV** switch at all times. If the simulation unit does not detect any activity from the **DATA ADV** switch it will automatically stop the simulation process after 999 axles.

Test Train Direction

The HBD front panel DIP switches determine the number of tracks in use, train direction, and format for speech annunciation. In this description direction is referred to as zero and one for the simulation unit. Direction zero is used when the **DATA ADV** switch is pressed once. Direction one is used when the **DATA ADV** switch is pressed twice, once to start the simulation and second time to reverse train direction.

Analog Board Circuits Used for Train Simulation

The following sections refer to several of the analog board circuits which are used in train simulation. The analog board DACs are used in all phases of train simulation. IC16(U5) is used to simulate the advance and gating transducer signals. The IC directs the DACs to advance/gating transducer circuits. IC29(U29) is used for simulating heat signals. The IC directs the DACs to the peak hold circuits.

Note: The operations specified for each state refer to both analog boards if system has been configured as a Hot Wheel detector with two analog boards. For example, when DAC1 and DAC2 are used for heat simulation (channel 1 and 2), DAC3 and DAC4 (on second analog board) are also used for heat simulation (channel 3 and 4).

Software Interface:

The HBD software is divided into two separate independent units, one which generates the signals to simulate the test train, and the other which process the signals as if a real train is passing the detector. The simulation unit is described here. The simulation unit uses time delays to simulate axle spacings, and speed of test train. These delays are also necessary, to give the simulated signals enough time to settle.

The simulation unit performs its task in 14 states. There is a delay between execution of each state. The delay introduced depends upon the speed of train. The following lists the delays for each type of train:

Slow trains	Delay of 10.0 ms
Medium trains	Delay of 5.0 ms
Fast trains	Delay of 2.5 ms

Other delays are used for simulation in other areas. The local delays vary for each state and will be explained as they are used. The global delays listed above, however, are constant during simulation.

State zero is responsible for the initial housekeeping. This state is executed only once upon activation of DATA ADV switch.

State 1, 2, 3, and 4 generate the advance transducer signals, signaling the processing unit to perform its pre train integrity test. These states are also executed after the 2 second wait period (change of direction by pressing the DATA ADV switch).

State 5 through 11 simulate the gate transducer signals, heat values using the DACs on analog board, and auxiliary alarms. These states are repeated as needed, 172 times for functional self test and as needed for the continuous test train.

State 12 and 13 simulate signals for the second advance transducers. They are also executed only once.

State 14 drops the track circuit, forcing the HBD to enter its End Of Train Timeout.

STATE 0: Housekeeping

Upon activation of the DATA ADV switch (if MODE switch is set to the "FUNCTIONAL SELF TEST" position, or position "E"), the HBD starts the simulation of test train by entering state zero. During this state the simulation unit waits for 2 seconds while monitoring the DATA ADV switch. All test trains have the same default direction. However, during the 2 second wait period, every time the DATA ADV switch is pressed, the simulation unit reverses direction of the train. State zero also forces the pre train integrity test to the result of previous 2 minute integrity test. The system integrity depends not only on the status of the pre-train integrity test for the current train, but also the previous two minute integrity test. This principle applies for real trains also.

STATE 1: Train is Approaching

State one activates the track circuit signaling the processing unit that a train is approaching. The presence of a train is accomplished by grounding the bit 2 on port 1 of digital board (TB12-3, track circuit input). There is a delay of approximately 3 milliseconds before the track circuit input is simulated. After simulation of the track circuit has occurred state one forces a local delay allowing the signal to settle down and the processing unit to perform its pre-train housekeeping. The local delay is:

Slow train	8 seconds
Medium train	4 seconds
fast train	2 seconds

State one then passes the control to state two. Note: The global delay mentioned previously which is forced before execution of each state applies here.

STATE 2: Advance Transducer Positive Pulse

State 2 simulate the positive pulse of the advanced transducer, while state 3 simulates the negative pulse. Direction of the test train determines which advance transducer is simulated. The positive pulse is generated by using the analog board DACs.

At first, state two inhibits the analog board 16/1 multiplexer, by setting port 5 to 100xxx10. P5.1 inhibits IC29(U29), while P5.7 inhibits IC16(U5).

Depending on the direction of the test train one of the DACs will receive a value of FF Hex (positive pulse), while the other will receive zero. If direction zero is used (DATA ADV was pressed only once) DAC1 is at FF, and DAC2 at zero. For direction one (DATA ADV was pressed twice), DAC1 is at zero, while DAC2 is at FF hex. After writing the proper values to the DACs (FF40 is DAC1, FF41 is DAC2), state two enables the multiplexer, directing its output to the advance transducer circuitry. Port 5 is modified to 011xxxxx. P5.7 enables IC16(U5), while P5.5 and P5.6 point DACs to the advance transducer A, using IC16(U5).

STATE 3: Advance Transducer Negative Pulse

State 3 simulates the negative pulse for the advance transducer. A value of zero is written to both analog board DACs regardless of train direction, simulating the negative pulse across the advance transducer. The state 3 algorithm is the same as the previous state when writing to analog DACs (the only difference is writing zero instead of FF hex to DACs). Refer state 2 for more information on how the DACs, and multiplexers are used.

Although state two and three simulate advance transducer signals they are executed only once (state 12 and 13 which simulate the other advance transducer signal are executed once also). Although in real train operation the number of advance transducer signals is equal to gating signals, the test trains only generate one signal for each advance transducer. The fact that the advance count and the gate counts are not equal does not effect train integrity.

STATE 4: Wait State

State 4 introduces a local delay for the processing unit to accomplish its pre-train integrity test and other housekeeping operations (this is the advance transducer start, approximately 200 ft). The local delay is:

Slow train	200 millisecond
Medium train	100 millisecond
Fast train	50 millisecond

This delay is not same as the global delay between execution of states.

State one and state four perform the same task. Both inform the processing unit that a train is approaching. While state one uses the track circuit method, state four uses the advance transducer method. The presence of both states make the test train simulation compatible for both system configuration.

STATE 5: Simulation of Auxiliary Alarms

State 5 simulates the predefined auxiliary alarms for the functional self test train. It also introduces delays between the simulated axles.

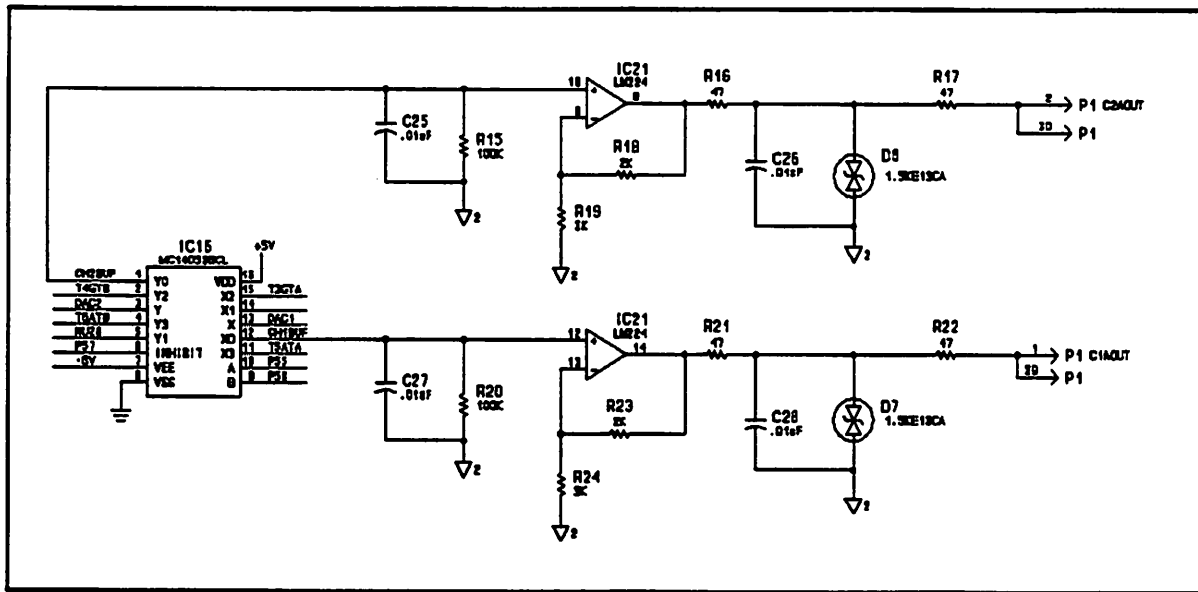
State 5 introduces a local delay equal to a predefined value. The table of delay values is given at the end of this section. The local delays introduced in this state and the following states simulate the time interval between axles. By changing the predefined delay values, new type of cars/locomotives, and train speed can be simulated.

After the local delay state 5 modifies the alarm port value (port zero of digital board). If the current axle has a pre-defined auxiliary alarm (specified in the table), the specific input on the alarm port is grounded. Note: Bit zero and one of this port are not used for alarm inputs. For more information on AUX alarm inputs refer to "Digital I/O" section of this document. Writing

to the digital board port 0 is only performed for functional self test trains. In the case of a continues test train, modification of the alarm port is by-passed.

STATE 6: Gate Transducer 1, Positive Pulse

State 6 simulates a positive pulse for the first wheel gate transducer. The train direction determines which gate transducer receives the positive pulse. For direction zero, DAC1 receives the positive pulse (FF Hex) while DAC2 remains at zero (reverse for direction one).



Like the other states, simulating the signal is done via the analog board DACs. First the 16/1 multiplexer is inhibited. By modifying port 5 of the analog board to 100xxx10, IC 29(U29) is inhibited (P5.1). IC16(U5) is also inhibited by P5.7.

After writing the proper values to DACs, port 5 is modified to xxxx. P5.7 enables IC16(U5), while P5.5 and 5.6 point the DACs to the gate transducers using IC16(U5).

STATE 7: Gate Transducer 1, Negative Pulse

State 7 writes a value of zero to both analog DACs simulating the negative pulse for the first wheel gate transducer. Operation of state 7 is similar to state 6. Port 5 is first modified to 100xxx10 to inhibit multiplexers and IC16(U5), and then modified to 010xxxxx to enable IC16(U5) and points the DACs to wheel gate transducer A.

STATE 8: Simulation Heat Signals

As described in the "SCANNER HEAT" portion of this document, the reference shutters are opened at this point (interrupts from state 6 open the reference shutters). The simulation unit generates the proper signals for channel 1, 2, 3, and 4 at this time.

In the case of a functional self test train, heat signals are based on predefined values which are listed at the end of this section. DAC1 and DAC2 represent channel 1, and 2. DAC3 and DAC4 are only used if the HBD has been configured as a Hot Wheel detector. For a continuous test train the actions listed in the next paragraph are by-passed. Note: A heat source can be placed in front of the scanners for a continuous train to induce heat values.

Port 5 is first modified to 100xxx10 to inhibit the multiplexers and IC16(U5). P5.1 inhibits the IC29(U29), while P5.7 inhibits IC16(U5).

Port 5 is then modified to xxxxxx01. P5.1 enables IC29(U29), pointing the DACs outputs to the peak hold circuit. At this point DACs receive their proper value (DAC1 is at FF40, DAC2 is at FF41).

The global delay between state 8 and 9 will give enough time to the peak hold circuit to charge to DACs values. Next state will generate the interrupt for the processing unit to start its AD conversion.

STATE 9: Gate Transducer 2, Positive Pulse

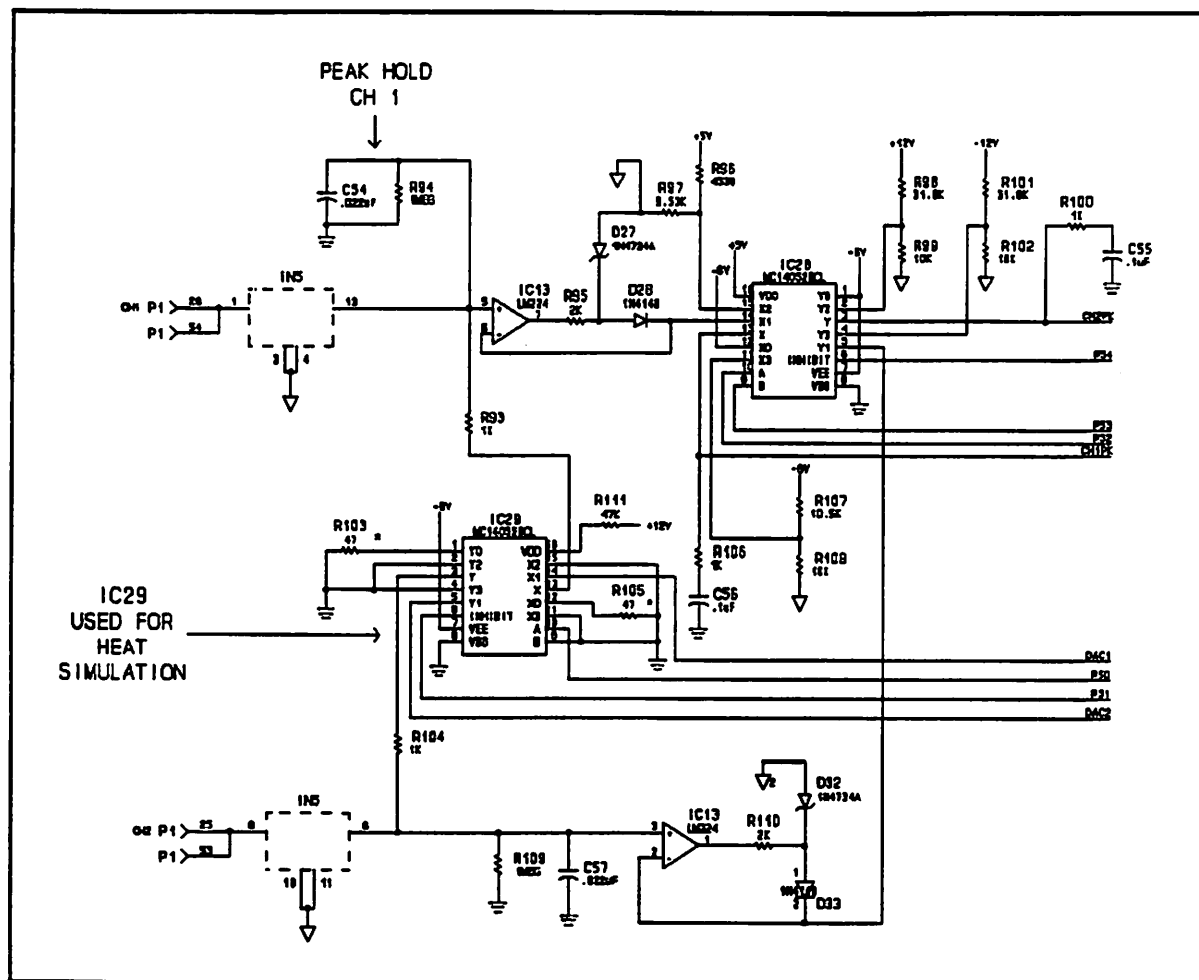
State 9 provides the positive pulse for the second wheel gate transducer. Generating the positive pulse at this point forces the processing unit to close the optical shutters and process the heat signals via the preamplifier and peak hold circuits.

DAC1 and DAC2 are used to simulate the positive pulse for the second wheel gate transducer (same as state 6). The values written to the DACs depend upon the train direction. However, if DAC1 received the FF value during state 6, it will remain at zero during this state, while DAC2 receives the FF hex value. Refer to state 6 for more information on how the analog board circuits are used to generate the positive pulse.

STATE 10: Gate Transducer 2, Negative Pulse

State 10 simulates the negative pulse for the second wheel gate transducer. As previously described, the simulation unit uses the zero value for the negative pulse. Thus DAC1 and DAC2 will both be at zero at this point (at this point, the optical shutters have been closed and the heat signals are being processed). Refer to state 6 for an explanation on how the DACs are use to generate the gating pulse.

At this point state 10 determines if the end-of-train has been reached. In the case of functional self test trains, the end of the table determines the end of the train. In the case of a continuous



test train, however, the status of DATA ADV switch is monitored. If the switch has been pressed or 999 axles have been simulated the end of the train is reached.

If the end of the train has been reached, control is passed to state 11. However if there are more axles to be generated, control is passed to state 5 to simulate the next axle.

STATE 11: Wait State

State 11 introduces a local delay simulating end of train before the last advance transducer is hit.

STATE 12: Second Advance Transducer Positive Pulse

State 12 simulates the positive pulse for the second advance transducer. The direction of a test train determines which advance transducer is simulated. For direction zero DAC1 is at zero, while DAC2 is at FF hex. For direction one, however, DAC1 is at zero while DAC2 will receive FF hex. Refer to state 4 for detailed information on how the DACs are used.

STATE 13: Advance Transducer Negative Pulse

State 13 simulates the negative pulse for the second advance transducer. A value of zero is written to both analog board DACs regardless of train direction, simulating the negative pulse across the advance transducer. The state 13 algorithm is the same as the previous state when writing to the analog DACs. The only difference is writing zero instead of FF hex.

STATE 14: End of Train

At this point, the processing unit has entered the "TIMEOUT" period. State 14 turns the track circuit off.

Functional Self Test Pre-defined Values:

The simulation unit uses the following table to generate the axle spacings (in form of local delays), heat signals, and auxiliary alarms. The table is made up of 172 lines, each having 8 fields. Each line is used to simulate an axle.

The first field is the axle number.

The second field of each line represents the auxiliary alarm inputs. The aux alarm byte is bit-encoded as follows:

Bit 0 (LSB)	: Not Used.
Bit 1	: Not Used
Bit 2	: Aux 1
Bit 3	: Aux 2
Bit 4	: Aux 3
Bit 5	: Aux 4
Bit 6	: Aux 5
Bit 7	: Not used.

The third byte represents Channel 1 heat.

The fourth byte is the Channel 2 heat.

The fifth byte is the Channel 3 heat.

The sixth byte is the Channel 4 heat.

The seventh byte is the distance to next axle. Each count in the distance field is approximately 4 inches. The distance between axles might differ for slow, medium, and fast trains. This is due to the local delays which simulate the distance between axles, and the interrupt structure of the HBD system. The simulation unit works on a 2.5 millisecond interrupts which is a high resolution for accurate distances.

The eighth field is the comment field. This field shows which car each axle belongs to and also identifies the alarms for each axle.

The heat values shown in the table are in a hexadecimal format. The HBD uses the Most Significant Bit as a sign bit. Thus the magnitude is only 7 bits long (0-127). The MSB is one

for positive values, and zero for negative values. The HBD strips off the MSB to process the heat value. For example, 08FH hex given in the table actually represents 15 (0FH) units after HBD strips the MSB. For this example the 08FH hex simulates a 3 millimeter heat pulse.

Cnt	Aux	Ch1	Ch2	Ch3	Ch4	Dist.	Comments
							CAR 1 (6 axle locomotive)
1		00H, 08FH, 08CH, 090H, 091H,	9				
2		00H, 08AH, 089H, 08EH, 08FH,	9				
3		00H, 08AH, 08AH, 08FH, 090H,	63				
4		00H, 08CH, 08FH, 08FH, 090H,	9				
5		00H, 089H, 090H, 08FH, 091H,	9				
6		00H, 089H, 08EH, 08FH, 094H,	27				
							CAR 2 (6 axle locomotive)
7		00H, 08FH, 090H, 093H, 098H,	9				
8		00H, 08BH, 08DH, 08FH, 094H,	9				
9		00H, 08AH, 08BH, 08FH, 096H,	63				
10		00H, 089H, 088H, 090H, 094H,	9				
11		00H, 08AH, 08CH, 090H, 096H,	9				
12		00H, 08BH, 08EH, 08FH, 094H,	27				
							CAR 3 (4 axle locomotive)
13		00H, 09DH, 09DH, 090H, 094H,	13				
14		00H, 099H, 09CH, 091H, 096H,	61				
15		00H, 090H, 097H, 08FH, 094H,	13				
16		00H, 097H, 096H, 090H, 097H,	27				
							CAR 4 (4 axle car)
17		00H, 099H, 0A4H, 090H, 092H,	5				
18		00H, 093H, 09DH, 08FH, 093H,	73				
19		00H, 09CH, 09CH, 092H, 08FH,	5				
20		00H, 09FH, 09CH, 093H, 08FH,	19				
							CAR 5 (4 axle car)
21		00H, 0FDH, 0C6H, 096H, 0FBH,	5	HW2, HB2			
22		00H, 099H, 099H, 096H, 0F9H,	73	HW2			
23		00H, 094H, 099H, 096H, 0FDH,	5	HW2			
24		00H, 0ACH, 094H, 096H, 0FDH,	19	HW2			
							CAR 6 (4 axle car)
25		00H, 098H, 094H, 08FH, 093H,	5				
26		00H, 09FH, 097H, 093H, 090H,	73				
27		00H, 09BH, 099H, 091H, 093H,	5				
28		00H, 098H, 09EH, 08FH, 092H,	19				

29 00H, 0C6H, 0C6H, 090H, 092H, 5
 30 00H, 0C6H, 0C6H, 093H, 093H, 73
 31 00H, 0C6H, 0C6H, 091H, 093H, 5
 32 00H, 0C6H, 0FDH, 08FH, 093H, 19 HB2

CAR 7 (4 axle car)

33 00H, 095H, 096H, 091H, 093H, 5
 34 00H, 092H, 098H, 093H, 08FH, 73
 35 00H, 099H, 09DH, 090H, 093H, 5
 36 00H, 091H, 099H, 08FH, 092H, 19

CAR 8 (4 axle car)

37 00H, 095H, 094H, 090H, 092H, 5
 38 00H, 09EH, 09BH, 090H, 092H, 73
 39 00H, 09CH, 097H, 090H, 092H, 5
 40 00H, 09DH, 08FH, 090H, 092H, 19

CAR 9 (4 axle car)

41 00H, 09CH, 09FH, 090H, 092H, 5
 42 00H, 09FH, 09FH, 090H, 092H, 73
 43 00H, 09FH, 09AH, 090H, 092H, 5
 44 00H, 096H, 09FH, 090H, 092H, 19

CAR 10 (4 axle car)

45 00H, 09FH, 097H, 093H, 093H, 5
 46 00H, 09FH, 09FH, 090H, 092H, 73
 47 00H, 09AH, 09AH, 093H, 08FH, 5
 48 00H, 0ACH, 098H, 092H, 08FH, 19

CAR 11 (4 axle car)

49 00H, 093H, 09AH, 090H, 092H, 5
 50 00H, 092H, 09EH, 093H, 08FH, 73
 51 00H, 092H, 093H, 092H, 092H, 5
 52 00H, 09FH, 093H, 093H, 08FH, 19

CAR 12 (4 axle car)

53 00H, 08FH, 093H, 095H, 094H, 5
 54 00H, 09EH, 094H, 095H, 094H, 73
 55 00H, 08FH, 093H, 095H, 094H, 5
 56 00H, 095H, 094H, 095H, 092H, 19

CAR 13 (4 axle car)

57 00H, 091H, 094H, 090H, 092H, 5
 58 00H, 097H, 098H, 091H, 093H, 73

CAR 14 (4 axle car)

59 00H, 098H, 095H, 08FH, 093H, 5
 60 00H, 097H, 098H, 090H, 092H, 19

CAR 15 (4 axle car)

61 00H, 093H, 095H, 095H, 097H, 5
 62 00H, 098H, 094H, 095H, 097H, 73
 63 00H, 097H, 090H, 090H, 092H, 5
 64 00H, 098H, 090H, 090H, 092H, 19

CAR 16 (4 axle car)

65 00H, 08AH, 08AH, 090H, 092H, 5
 66 00H, 08AH, 08CH, 090H, 092H, 73
 67 00H, 08DH, 08DH, 090H, 092H, 5
 68 00H, 088H, 088H, 090H, 092H, 19

CAR 17 (4 axle car)

69 00H, 099H, 097H, 090H, 092H, 5
 70 00H, 09AH, 097H, 090H, 092H, 73
 71 00H, 093H, 093H, 090H, 092H, 5
 72 00H, 09DH, 093H, 090H, 092H, 19

CAR 18 (4 axle car)

73 00H, 094H, 09AH, 095H, 095H, 5
 74 00H, 09DH, 09DH, 095H, 097H, 73
 75 00H, 097H, 098H, 086H, 092H, 5
 76 00H, 09AH, 09EH, 08AH, 092H, 19

CAR 19 (4 axle car)

77 00H, 08FH, 08FH, 08BH, 08FH, 5
 78 00H, 099H, 09FH, 08AH, 08AH, 73
 79 00H, 094H, 09CH, 08BH, 08AH, 5
 80 00H, 09AH, 09EH, 08CH, 092H, 19

CAR 20 (4 axle car)

81 00H, 092H, 092H, 092H, 092H, 5
 82 00H, 092H, 094H, 092H, 092H, 73
 83 00H, 090H, 098H, 090H, 090H, 5
 84 04H, 099H, 09DH, 091H, 093H, 19

AUX1

CAR 21 (2 axle car)

85 04H, 094H, 092H, 091H, 093H, 73
 86 04H, 09BH, 09AH, 094H, 08FH, 19

AUX1

AUX1

87	08H, 084H, 082H, 08FH, 092H, 73	AUX2	CAR 22 (2 axle car)
88	00H, 0D4H, 08FH, 08EH, 092H, 39	HBD1	
89	00H, 09BH, 098H, 08AH, 08DH, 5		CAR 22 (4 axle car)
90	00H, 0A8H, 096H, 094H, 092H, 73		
91	10H, 08FH, 094H, 093H, 08FH, 5	AUX3	
92	10H, 093H, 097H, 08FH, 092H, 19	AUX3	
93	00H, 091H, 091H, 090H, 092H, 5		CAR 23 (4 axle car)
94	00H, 098H, 098H, 090H, 092H, 73		
95	20H, 090H, 090H, 090H, 092H, 5	AUX4	
96	20H, 094H, 094H, 090H, 092H, 19	AUX4	
97	00H, 094H, 093H, 08FH, 097H, 5		CAR 24 (4 axle car)
98	00H, 0A3H, 09AH, 08FH, 097H, 73		
99	00H, 09AH, 094H, 08FH, 095H, 5		
100	00H, 09AH, 09BH, 08FH, 094H, 19		
101	00H, 09AH, 099H, 08FH, 092H, 5		CAR 25 (4 axle car)
102	40H, 094H, 098H, 08FH, 092H, 73	AUX5	
103	40H, 09DH, 094H, 08FH, 092H, 5	AUX5	
104	00H, 090H, 094H, 092H, 092H, 73		
105	00H, 098H, 093H, 090H, 092H, 5		CAR 26 (4 axle car)
106	00H, 097H, 097H, 090H, 092H, 73		
107	00H, 093H, 095H, 090H, 092H, 5		
108	00H, 096H, 09BH, 090H, 092H, 19		
109	00H, 087H, 088H, 0A3H, 0A1H, 5		CAR 27 (4 axle car)
110	00H, 089H, 084H, 09CH, 0A1H, 73		
111	00H, 089H, 08DH, 09AH, 09CH, 5		
112	00H, 08EH, 08EH, 09AH, 0A1H, 73		
113	00H, 0A2H, 0A2H, 090H, 092H, 5		CAR 28 (4 axle car)
114	00H, 0A3H, 0B4H, 090H, 092H, 73		
115	00H, 09DH, 098H, 090H, 092H, 5		
116	00H, 0A9H, 0B2H, 090H, 092H, 19		

CAR 29 (4 axle car)

117 00H, 09DH, 09BH, 090H, 092H, 5
 118 00H, 094H, 09AH, 090H, 092H, 73
 119 00H, 09AH, 099H, 090H, 092H, 5
 120 00H, 095H, 095H, 090H, 092H, 73

CAR 30 (4 axle car)

121 00H, 08CH, 086H, 086H, 088H, 5
 122 00H, 08CH, 087H, 08BH, 08DH, 73
 123 00H, 088H, 086H, 08BH, 088H, 5
 124 00H, 088H, 08AH, 08BH, 097H, 19

CAR 31 (4 axle car)

125 00H, 09BH, 097H, 090H, 092H, 5
 126 00H, 09CH, 097H, 092H, 092H, 73
 127 00H, 093H, 097H, 092H, 092H, 5
 128 00H, 095H, 09AH, 092H, 092H, 73

CAR 32 (4 axle car)

129 00H, 097H, 094H, 090H, 092H, 5
 130 00H, 09DH, 09DH, 090H, 092H, 73
 131 00H, 093H, 093H, 090H, 092H, 5
 132 00H, 090H, 097H, 090H, 092H, 19

CAR 33 (4 axle car)

133 00H, 09CH, 099H, 092H, 093H, 5
 134 00H, 093H, 09BH, 091H, 093H, 73
 135 00H, 096H, 096H, 091H, 093H, 5
 136 00H, 09FH, 096H, 091H, 092H, 73

CAR 34 (4 axle car)

137 00H, 096H, 09AH, 090H, 092H, 5
 138 00H, 09FH, 09DH, 091H, 092H, 73
 139 00H, 09AH, 097H, 092H, 092H, 5
 140 00H, 09FH, 093H, 091H, 092H, 19

CAR 35 (4 axle car)

141 00H, 091H, 09AH, 090H, 092H, 5
 142 00H, 09CH, 09AH, 090H, 092H, 73
 143 00H, 09FH, 097H, 090H, 092H, 5
 144 00H, 09DH, 091H, 090H, 092H, 73

CAR 36 (4 axle car)

145 00H, 09FH, 098H, 095H, 092H, 5
 146 00H, 093H, 092H, 095H, 092H, 73

147 00H, 09FH, 09BH, 095H, 092H, 5
 148 00H, 09CH, 098H, 095H, 092H, 19

CAR 37 (4 axle car)

149 00H, 097H, 09AH, 090H, 092H, 5
 150 00H, 097H, 09AH, 090H, 092H, 73
 151 00H, 09FH, 097H, 090H, 092H, 5
 152 00H, 09EH, 097H, 090H, 092H, 73

CAR 38 (4 axle car)

153 00H, 099H, 09FH, 09AH, 09CH, 5
 154 00H, 099H, 099H, 09AH, 097H, 73
 155 00H, 09DH, 093H, 095H, 09CH, 5
 156 00H, 09FH, 09EH, 095H, 09CH, 19

CAR 39 (4 axle car)

157 00H, 097H, 09EH, 095H, 092H, 5
 158 00H, 09EH, 09EH, 095H, 092H, 73
 159 00H, 095H, 095H, 095H, 092H, 5
 160 00H, 09CH, 09EH, 095H, 092H, 73

CAR 40 (4 axle car)

161 00H, 09AH, 098H, 090H, 097H, 5
 162 00H, 093H, 094H, 090H, 097H, 73
 163 00H, 099H, 094H, 090H, 097H, 5
 164 00H, 098H, 098H, 090H, 097H, 19

CAR 41 (4 axle car)

165 00H, 099H, 094H, 093H, 093H, 5
 166 00H, 099H, 09FH, 091H, 093H, 73
 167 00H, 09AH, 090H, 093H, 092H, 5
 168 00H, 09DH, 097H, 093H, 092H, 73

CAR 42 (4 axle car)

169 00H, 096H, 09AH, 08FH, 08FH, 5
 170 00H, 08CH, 09AH, 08FH, 094H, 73
 171 00H, 098H, 097H, 08FH, 092H, 5
 172 00H, 09BH, 0E5H, 092H, 097H, 0

HB2

Chop Mode

Main Boards Utilized

ANALOG AND UNIVERSAL PROCESSOR BOARDS

Theory of Operation

The "Chop" mode is used during the installation, calibration, alignment, and maintenance of the hot box detector scanners and associated circuitry. The main function of "Chop" is to verify that scanners are reading an appropriate amount of heat from a known heat source. For proper system calibration, a calibrated heat source is required for scanners manufactured by Harmon Electronics, Inc. and a function simulator/generator is required for scanners manufactured by Servo Corporation of America.

The CHOP mode is started by placing the MODE switch in position "B". The DATA DISPLAY will show "*CHOP*" if scanners manufactured by Harmon Electronics, Inc. are installed or "-CHOP-" if scanners manufactured by Servo Corporation of America are installed. Pressing the DATA ADVANCE switch initiates a series of continuous simulated wheel gates. Heat values read at the scanners are displayed on the DATA DISPLAY in the form of "CHn=xx.x", where 'n' is a channel number and 'x' is a decimal digit. The heat displayed on the DATA DISPLAY is in millimeters. If a chart recorder is installed, the heat displayed is a graphical representation in millimeters. Pressing the DATA ADVANCE switch again steps through the attached scanners. The CHOP mode can be reset in one of three ways. Those are by pressing the RESET switch, the presence of a real train, and the MODE switch being placed in another position.

Software Interface

When the "Chop" mode is initiated through the above procedure a flag is set in the main program that passes control to the "Chop" software. The "Chop" software is executed through a 2.5 millisecond interrupt. The controlling flag is monitored and updated on the main 50 millisecond program loop.

There are two variations of the "Chop" program: one is used when interfacing to Model 33 and Model 3300 scanners and the other is used for Servo scanners. These two different programs do, although share some common routines such as displaying heat on the DATA DISPLAY. This description will cover the common routines first and then will cover the routines that depend on the scanner type.

Common Routines

Every time the "Chop" program is called the DATA ADV is monitored for activity. If the DATA ADV is never pressed the DATA DISPLAY shows the "Chop" headers as described above and the system constantly prepares the environment to start reading heat samples. When the DATA ADV is pressed the DATA DISPLAY changes to "CH1=xx.x" where x is the heat reading in

millimeters. Pressing the **DATA ADV** a second time changes the **DATA DISPLAY** to "CH2=xx.x". Pressing the **DATA ADV** after this simply changes the channel being displayed by one. If a hot wheel scanner is installed the channel display will go to "CH4=xx.x".

Model 33 and Model 3300 Scanners

The "Chop" mode can only be initiated when the main program is in the No Train Around mode of operation and the **MODE** switch is placed in position "B". Once "Chop" is entered it can be halted upon the approach of a real train, moving the **MODE** switch, or by pressing the **RESET** switch.

The chop program operates as a state machine consisting of 8 states. One state can be called every 2.5 milliseconds. Upon the completion of one state the next state is prepared to receive control. Following is a state by state description of the steps performed in each state:

1. The optical shutters are opened exposing the sensing device to the heat source.
The analog channel is connected to the peak hold circuit and prepared to obtain the next sample. For a more precise description of how the hardware interfaces to the software refer to the "Scanner Heat" section of this manual.
2. Keep opening the optical shutter.
3. Stop opening the optical shutter and begin charging the peak hold capacitor.
4. Keep charging the peak hold capacitor.
5. Stop charging the peak hold capacitor and perform an AD conversion of the voltage on the peak hold circuit.
Start closing the optical shutter.
After the voltage has been converted into a heat value display the results of the reading on the **DATA DISPLAY**. At the same time write the heat value on the chart recorder if installed.
Disconnect the peak hold circuit from the AD convertor.
6. Keep closing the optical shutter.
7. Stop closing the optical shutter.
A timer that causes the heat to be held on the chart recorder for at least 200 milliseconds is initiated.
8. Wait until the 200 millisecond has expired before repeating step 1. Step 1 through step 8 is repeated until the **MODE** is moved to another position or the **RESET** switch is pressed.

Servo Scanners

The "Chop" mode can only be initiated when the main program is in the No Train Around mode of operation and the **MODE** switch is placed in position "B". Once "Chop" is entered it can be halted upon the approach of a real train, moving the **MODE** switch, or by pressing the **RESET** switch.

The chop program operates as a state machine consisting of 3 states. One state can be called every 2.5 milliseconds. Upon the completion of one state the next state is prepared to receive control. Following is a state by state description of the steps performed in each state:

1. The analog channel is connected to the peak hold circuit and prepared to obtain the next sample. For a more precise description of how the hardware interfaces to the software refer to the "Scanner Heat" section of this manual.
2. Start charging the peak hold capacitor.
3. Perform an ADC to obtain the heat reading.

Servo scanners do not use an optical reference shutter to determine the ambient reference temperature. They use the underside of the car for ambient reference. During the "Chop" mode a Servo calibrator unit uses a spinning wheel with a hole in one spot that exposes the bolometer to the heat source for a short period of time in comparison to the time the bolometer is exposed to the "ambient reference." Because of this the software takes several samples and averages them together and displays the result of those samples.

The sampling makes the response time while in the "Chop" mode appear to be somewhat slower but the output to the chart recorder and the **DATA DISPLAY** is just as accurate as a system using Model 33 and Model 3300 scanners. Following is a description of the average algorithm and how the software controls the hardware:

- The average of the last four heat samples is computed with the oldest heat sample being discarded from the circular queue of 4 heat readings.
- If the new heat sample is greater than the current average the multiplexer, IC29(U29), is disabled. When the multiplexer is disabled the 51K Ω resistor is connected to ground, discharging the peak hold circuit. Wait for approximately 300 milliseconds before proceeding.
- Perform the above steps for the other channel.

- Write the last valid heat reading to the chart recorder. Display the heat reading on the **DATA DISPLAY** in the for "CHx=yy.y" where x is the current channel number and y is the heat value in millimeters.

Clear the analog channel to get ready for the next reading.

Wait for a few milliseconds and start charging the peak hold circuit again. Step 1 through step 3 is repeated until the **MODE** is moved to another position or the **RESET** switch is pressed.

Boards Self Test

Main Boards Used

ALL HBD BOARDS

Theory of Operation

The HBD software provides a board self-test which is used to test the integrity of the individual HBD circuits/boards. The board self test is a detailed testing procedure which is performed at the board level by running a sequence of tests on individual circuits of each board. The board self test is set up for two levels of examination. The first level tests the individual boards one by one giving the results in a general format (PASSED/FAILED). The second mode also examines the boards one by one but upon reaching a specific sub-test that fails the HBD display the name of the circuit that failed and repeats that test until the test passes or the **DATA ADV** switch is pressed to advance the test to its next stage.

The board self test is performed in 5 states (one per HBD board). Each state consists of several sub-tests which exercise the integrity of a specific circuit on the board.

The board self test described here is also a part of the integrity test performed every two minutes. In case of any failure a proper message is written to the chart recorder during end-of-train timeout and transmitted to DCP.

This section first explains how a board test is generated using the HBD front panel switches. The next section describes the testing of the individual circuits/components that are tested during the board self test along with technique used to test them. Note: The circuits/components of each board discussed here are only a portion of the board electronics for more information on the boards refer to the hardware description in this manual.

Starting Board Self Test

To start the board self test place the **MODE** switch to the **BOARD SELF TEST** position. The **DATA DISPLAY** should show the phrase "TEST?". If the **DATA DISPLAY** shows "INTEGRITY" the HBD is performing its two minute integrity test. You must wait for the HBD to finish its two minute integrity test before stating the board self test.

The **FUNCTION** switch is not used in the board self test. The **RESET** switch will cancel the board self test and the phrase "TEST?" will be displayed again. Upon arrival of a real train the board self test will automatically be canceled by the HBD.

The **DATA ADV** switch is used to start and control the board self test. If the **DATA DISPLAY** switch is pressed once the HBD performs the first level of testing (giving the PASSED/FAILED message for each board). To instruct the HBD to execute the second level of testing the **DATA ADV** switch must be pressed twice. While the HBD performs its board sub-tests it monitors the

DATA ADV switch. The switch can be pressed for the second time at any time. Upon pressing the **DATA ADV** for the second time the HBD performs the remaining sub-tests using the second level of testing.

First Level Test

To start the board self test place the **MODE** switch in the **BOARD SELF TEST** and press the **DATA ADV** switch.

The HBD displays the name of the board under examination (CPU, ROM, ANALOG, SPEECH, DIGITAL). Once the test has been performed the HBD displays the "PASSED" phrase if the board passes all the sub-tests and "FAILED" if any of the sub-tests fails. The HBD then tests the next board displaying the results in the same fashion. After all the boards have been tested the HBD displays "FAILED" if any of the boards failed their test and "PASSED" otherwise.

Second Level Test

To start the second level of board self test the **DATA ADV** switch must be pressed twice. At this level the HBD displays the name of the board prior to examining the board. Board sub-tests are then performed to test the integrity of the board (circuits). If the board passes all the sub-tests the HBD displays the phrase "PASSED" and starts the next board. If one of the sub-tests fails however, the HBD displays a proper message (name of the circuit or component) and repeats the same sub-test over. The sub-test is repeatedly performed by the HBD until the cause of failure disappears or the **DATA ADV** switch is pressed, advancing the test to the next state. The **DATA ADV** switch is used to manually advance the board self test. For example if one of the auxiliary inputs is stuck the digital board test (port sub-test) will re-examine the specific port until the stuck input has been repaired or the **DATA ADV** switch is pressed.

When all the boards have been tested the HBD displays the phrase "FAILED" if any of the circuits failed their test and "PASSED" if all of the tests have passed.

1. CPU Board Test

The Universal Processor (CPU) board is the brain of the HBD system. The CPU board contains the following circuits which controls every aspect of the HBD operation.

- * Micro-controller (8031) chip; which is the brain of the CPU board. The micro-controller chip fetches the program instructions from the memory and executes them.
- * EPROMs; four Erasable Programmable Read Only Memory (EPROM) chips hold the HBD software which is custom programmed to meet the customers specific requirements.
- * RAMs; two Random Access Memory (RAM) chips which are used as scratch pad during run time by the HBD software.

* Address Lines

* Select Lines

The followings are the sub-tests performed at the first state of board self test. The Following sections describe each sub-test in more detail.

- 1 - Micro-controller (8031) internal circuits.
- 2 - Micro-controller internal registers.
- 3 - Micro-controller internal RAM.
- 4 - Software checksum EPROM0 EPROM1 EPROM2 EPROM3.
- 5 - Select lines for the two static RAMs on the CPU board.
- 6 - Address lines for the two static RAMs on the CPU board.
- 7 - Internal structures (Flip Flops) of both static RAMs.

1.1 Micro-controller Internal Circuits

This sub-test consists of four steps. Each step performs an operation with known operands/results and a checks those results. The four tests examine integrity of ALU(Arithmetic Logic Unit) the A and B registers and the CPU carry and overflow flag.

The Arithmetic Logic Unit of the 8031 (ALU) as the name indicates performs all the arithmetic (add subtract multiply divide..) and logic (AND OR shift rotate..) operations.

The 8031 micro-controller is an accumulator based processor. This means that for any operation the accumulator (A register) must hold at least one of the operands. The B register is an internal scratch pad register. For some operations (multiply, divide) the B register holds one of the operands. The Carry Flag is set if the operation results in a carry out of (addition) or a borrow into (subtraction) the high order bit of the result; otherwise the carry flag is cleared. The Overflow Flag is set if the operation results in a carry into the high order bit of the result but not a carry out of the high order bit or vice versa; otherwise the overflow flag is cleared.

Each test exercises two features of the circuits. First if the CPU internal circuits perform correctly and second if the flip flops which construct the registers and flags keep their values (bit holding power).

Testing the micro-controller internal circuits consists of two multiplications two divisions and several logic operations (AND OR OR shift bits rotate with/without carry).

For each operation, since the operand(s) are known, the results are checked against a known value. If a failure is encountered the HBD displays a proper message on the **DATA DISPLAY** and bypasses the rest of operations. For a complete list of circuit failures refer to end of this section.

1.2 Micro-controller Internal Registers

The previous state tested three of the 8031 registers (A,B and flag registers). At this state the HBD tests the remaining internal registers of the 8031 micro-controller (PSW DPTR IP IE) and the timer group.

The Program Status Word (PSW) is an eight bit (8 flags) register which records the processor status information and controls the operation of the processor. The Data Pointer (DPTR) is used in register-indirect addressing to move program memory constants, external data memory variables, and to branch to specific memory address space. The Interrupt Enable (IE) register can be programmed to disable/enable any one of the 8031 5 interrupts. The Interrupt Priorities (IP) determines which interrupts have the higher priorities. The 8031 also contains two 16 bit timers which are used by the HBD software to manage its tasks.

The only test performed on the registers is the bit holding test. Each register is loaded with three different values (00H, 0FFH, and 077H). After a short delay the register value is read and tested against the specific value. If the test is successful the next sub test is performed. If a failure is encountered a proper message is displayed on the **DATA DISPLAY** and the remaining sub tests are by passed.

After testing the registers for their bit holding power the timer groups are examined. Here the HBD tests the two timers on the CPU chip against themselves. Timer one is set to time out before timer zero is ready to time out. When timer one times out the timers are stopped and timer zero is checked to insure that it is within range. This sub-test makes sure neither timer times out too quickly or too slowly

1.3 Micro-controller Internal RAM

8031 micro-controller contains 128 bytes of internal data memory. The lowest 32 bytes are grouped into 4 banks of 8 registers. The next 16 bytes form a block of bit-addressable memory space. The 128 byte RAM is involved in almost all the HBD operations. This space must always be in a proper condition.

This portion of the test examines the bit holding power of the data memory space. The interrupts are first disabled so that other HBD tasks will not interfere with the test. Each memory location is first read in then complemented and stored back in the same location. After a short delay the new value is read again and compared to the expected value. If they differ the test has failed and a proper message is written to **DATA DISPLAY** otherwise the next byte will be tested.

1.4 Software Checksum EPROM0 EPROM1 EPROM2 EPROM3

The 4 Erasable Programmable Read Only Memory (EPROM) contain the HBD software to meet specific requirements. When programming the EPROMs a checksum of data contained in each EPROM is written to the last two locations of EPROM space.

To test the integrity of the HBD software this portion of test re-calculates the checksum for each EPROM and compares the value to the stored checksum. If they differ the checksum test has failed, otherwise same test will be performed for the next EPROM.

1.5 Select Lines for the Two Static RAMs on the CPU Board

The CPU board contains two static RAM chips. This portion of the test examines the RAM select lines while the next test examines the RAM address lines.

The value stored in the same location (same address) on both RAMs are read and compared. If they contain different data then the RAM select lines are working properly. However, if the values from the RAMs are the same, a new value is written to the same location on RAM 0. After a short delay the same locations (on both RAMs) are once again read and compared. At this point both values must be different otherwise the select lines are not working properly.

Note: Before performing these sub-tests the interrupts are disabled so that no HBD task can modify the memory location under test. The original values are saved using the stack before the test and written back after the test.

1.6 Address Lines for the Two Static RAMs on the CPU Board

This sub-test examines the two RAM chips on the CPU board for stuck address lines. Each address line when toggled must access a different location.

First, the value stored in the first location (memory space) is read. The address lines are then complemented and the value for the second location is read. If the two values are different the address lines have selected two different locations. However if the values are the same a new value is written to the second location after which the above procedure is repeated once again. At this point however the values of two location must be different or the address lines are at fault.

This procedure is performed for all the addressable bytes on the RAMs (128 bytes).

1.7 Internal Structures (Flip Flops) of Both Static RAMs

This sub-test examines the bit holding power of both RAMs on the CPU board. For each byte of data memory space the value is read and complemented. The new value is written back to the same location. After a short delay the new value is read again and compared with the original value (its complement). Using this method each byte is tested to see if it can hold an assigned value.

2. ROM Board

The ROM board consists of several speech EPROMs which have been programmed for HBD message annunciation. Each EPROM consists of several words (phrases) stored digitally. The

speech board circuits reads the words in digital form and converts them to an analog form to generate HBD messages.

During the programming phase of the speech EPROMs a checksum is entered at the last two location of EPROMs. To examine the integrity of speech data the HBD recalculates the checksum for each EPROM and compares it to the checksum stored in the last two location. If the checksums are different the EPROM has been damaged and must be replaced.

If the second level of board self test is being executed the EPROM which failed will be displayed on the **DATA DISPLAY** (EPROM numbers start from zero).

3. Speech Board

3.1 Speech Board Port 2

This sub-test examines the capacitors which are a part of each bit in the port. It also detects bad OP Amps and transistors.

First a value of 055H is written to the port. After a short delay the port is read and compared to 055H. This determines if any of the output lines are shorted on the PC board. If the test was successful the procedure is repeated with 0AAH value. Here the set/clear bits are reversed.

Next the capacitors are examined. First a value of zero is written to the port. The HBD then forces a delay for the port to settle. At this point a value of 0FFH is written to the port. However only a short delay which is not long enough for port to settle is forced. At this point the port is read and compared to zero. Note: Since the port did not have enough time to settle the value must be zero and not 0FFH (or any other value except zero). If this sub-test passes the HBD repeats the procedure, however, this time HBD allows enough time for port capacitors to charge (settle). The port value at this time must be 0FFH since the port have had enough time to settle.

3.2 Speech Board Port Reset Capacitors

This sub-test examines the capacitor on the reset line that comes into the board. It is tested to make sure that the delay induced by the capacitor is within specified limits.

To make sure that the capacitor is within limits the HBD checks on either side of the "time window" which determines the acceptable range of performance. If it does not change too quickly or too slowly the capacitor is in proper condition. To detect this, the HBD looks at the outputs of port. When the reset line goes high the port should go to high impedance. If it goes to high impedance within the "time window" then everything is alright. To implement this, all zeros are written to the port reset line which is taken high and the port is checked twice. It should have time to change to high impedance or all 1's. If the port is not all zeros on the first test and all ones on the second test has failed.

4 Digital Board

4.1 Port 0 of Digital Board

The HBD software tests most of the port 0 components. The components tested are: the port capacitors/transistors, the XOR gates which are used for the polarity control, the storage Flip Flops, the bi-directional data buffer, the interrupt enable, the NAND gates, and the four latches (data output latch polarity control latch storage control latch and interrupt control latch).

The digital port 0 test begins by examining the capacitors and transistors. First, a value of zero is written to the port. The HBD then forces a delay for the port to settle. At this point a value of 0FFH is written to the port. However only a short delay, which is not long enough for port to settle, is forced. At this point the port is read and compared to zero. Note: The port does not have enough time to settle, the value must be zero. If this sub-test passes the procedure is repeated but the next time the HBD allows enough time for the port capacitors to charge (settle). The port value at this time must be 0FFH since the port have had enough time to settle.

The polarity control circuits (U15 and XOR gates U13 and U14) are then tested as follows:

- 1 - Read and store the contents of port 0.
- 2 - Set the polarity control for inverting data (0FFH to U15) which in turn leaves a logic one at the XOR inputs.
- 3 - Read port 0 again. At this point the two values are compared to test the integrity of the polarity control circuit.

The storage control circuit (U16 U18) is the next circuit tested. For this test the storage control latch is set for the "one time latch" mode (00H to U18). Port 0 is then read. Note: Port 0 must now be equal to 0FFH from previous test. Port 0 value is then compared to a known value (0FFH). For next step the storage control latch is set to dynamically follow the data (0FFH to U18). After resetting the polarity control latch to pass the data the unchanged port 0 value is read and tested for the proper value.

4.2 I/O Interrupts

The interrupt control latch (U21) and the interrupt enable/disable NAND gates are examined in this test. The interrupt port on the processor board is also indirectly tested.

To perform this test the polarity control latch (U21) is set to invert the incoming data, and the storage control latch (U22) is set to follow all data. The HBD then generates the inputs for an interrupt for each NAND gate. For example; at first, port zero bit 0 is set to one. The output of the XOR gate drives the U16 SR Flip Flop to create an interrupt using the NAND gates (U19). The HBD reads in the interrupt lines and compares the current active interrupt against bit zero of port 0. The above procedure is repeated seven more times (p0.1 to p0.7).

4.3 Port 1 of Digital Board

The operations performed are same as described in section 3.1. However port 1 of digital board is tested.

4.4 Port 2 of Digital Board

The operations performed are same as described in section 3.1. However port 2 of digital board is tested.

4.5 Reset Capacitor

Refer to section 3.2 (Speech Board Port Reset Capacitor) on the operation of this test. Note: This test is performed for port zero of the digital I/O board.

5. Analog Board

The analog board interfaces external analog devices and inputs to the digital portion of the HBD. The analog board also converts the digital signals from the CPU board to drive several devices. The analog board circuits which are examined during the board self test are as follow:

- * Analog to Digital Converters (ADCs)
- * Digital to Analog Converters (DACs)
- * Power Supplies
- * Peak Hold Circuit

The analog board test consists of several states. The following sections explain each state in detail. Note: All reference designators given are for analog II board while analog I board is given in (). The x in the bit patterns given means don't care.

5.1 Analog Board DAC 1, Analog Board DAC 2, Analog Board ADC

This test sets specific values into the DACs and reads them into the ADC. If the DACs and ADC agree then both the DACs and the ADC are good. However if a failure occurs one of the following conditions exists.

- a - DAC1 failed DAC2 OK. (ADC OK).
- b - DAC1 OK DAC2 failed. (ADC OK).
- c - DAC1 and DAC2 failed. In this case it is possible that the DACs are OK but the ADC (common in both tests) is bad. It is also possible that the ADC is OK and both DACs are bad.

The following steps describe how the DACs and the ADC are tested.

- 1 - Connect DAC1 to the ADC by setting the analog board port 6 to xxx01111. DAC1, which is x input of IC29(U29), is the input of the peak hold circuit which in turn will be the x input (and x output) of IC28(U25).
- 2 - Write a value of 10 to DAC1 (FF40).
- 3 - Start the AD conversion by setting the analog port 6 bit 5 to 1 (xx1xxxxx). A delay of a few clock cycles is used and then the bit 5 (bit 6.5 is the "start AD" input of ADC IC19(U21)) is cleared.
- 4 - Read AD value. The AD value is read from the analog board port 1. The HBD waits a maximum of 3.44 milliseconds for an interrupt from the AD converter (conversion successful). The interrupt comes in on bit 7 (1xxxxxxx) of the analog board port zero. If the AD conversion was not successful (no interrupts in 3.44 ms wait period) a value of zero is used for comparison.
- 5 - The original value (written to DAC) is now compared to the AD value. If the difference between the two values is 5 percent or less (than the full scale), test has passed. The test fails if the difference is greater than 5% of the full scale.

The above procedure is repeated 22 times. At first a value of 10 is written to DAC1. The value is then incremented by 10 for the next tested (values range from 10 to 250). Note: The DAC must pass all the test values to pass the test.

After finishing the DAC1 test a similar test is performed for DAC2. The only difference is connecting DAC2 to ADC. To connect DAC2 to the ADC the analog board port 6 receives xxx10111.

The results of both tests (DAC1 and DAC2) are then compared. As mentioned previously, the ADC is the common circuit in both tests. If one of the DACs failed, the ADC and the other DAC is in good condition, but if both tests failed either both DACs are bad or the ADC (common circuit) is BAD.

5.2 Power Supplies Test

The power supply test examines the four power supplies (+5 VDC -6 VDC +12 VDC -12 VDC) by using the ADC. As previously described, the board self test described here is also a part of the two minute integrity test. The same procedures and test values are used for all the board tests with the exception of the power supplies test. The pass criteria for the power supplies are different depending on whether an integrity test or a board self test is being executed. The values used are listed at the end of this section.

To perform the test HBD executes the following steps:

1 - IC28(U25) is used to point the power supply under test to the output (ch1_pk or ch2_pk) of the multiplexer IC28(U25). As shown ch1_pk can be used for the +5 VDC and -6 VDC (x inputs of the multiplexer) power supplies while ch2_pk can be used for the +12 VDC and -12 VDC (y inputs of multiplexer) power supplies. The analog board port 6, which controls the IC17(U26) and IC20(U27), is first modified to send the ch1_pk/ch2_pk output to the ADC. Port 6 is modified to xxx01000 for ch2_pk and to xxx10000 for ch1_pk (bits 6.0, 6.1, and 6.2 select the x0 input while bits 6.3 and 6.4 select one of the 8 to 1 multiplexers).

2 - The ADC is connected to the power supply under test by modifying the analog board port 5 which controls IC28(U25). For the +5 VDC (x input) and +12 VDC (y input) power supplies port 5 is modified to xxx010xx. For the -6 VDC (x input) and -12 VDC (y input) power supplies port 5 is modified to xxx011xx (bits 5.2 and 5.3 select the power supply input and bit 5.4 is the inhibit of multiplexer).

3 - Delay 6 milliseconds.

4 - Read the AD value. The AD value is read from the analog board port 1. The HBD waits a maximum of 3.44 milliseconds for an interrupt from the AD converter (conversion successful). The interrupt comes in on bit 7 (1xxxxxxx) of the analog board port zero (IC19(U21)). If the AD conversion was not successful (no interrupts in 3.44 ms wait period) a value of zero is used for comparison.

5 - Compare the ADC value to a predefined low and hi limit. If the value is within the "window" the power supply passes. The ranges for the board self test voltages are as follow:

Supply	Low	High
+5 VDC	+4.75	+5.25
-6 VDC	-6.60	-5.40
+12 VDC	+11.16	+12.84
-12 VDC	-13.20	-10.80

Ranges for integrity test voltages are as follow:

Supply	Low	High
+5 VDC	+4.65	+5.35
-6 VDC	-6.90	-5.10
+12 VDC	+10.80	+13.20
-12 VDC	-13.80	-10.20

5.3 Channel Peak Hold Zero Test

The peak hold zero test algorithm is as follows:

- 1 - Point the ADC to ch1_pk by modifying port 6 of the analog board (xxx10000). Bits p6.0, p6.1, p6.2, and p6.3 put the ch1_pk input of IC17(U26) to its output which is in turn the analog input of ADC (IC19(U21)). Ch1_pk is the x output of IC28(U25).
- 2 - The ch1_pk x output of IC28(U25) is connected to -6 VDC by setting port 6 of the analog board to xxx000xx. As shown, p5.2 and p5.3 connect the x0 input (-6 VDC) to the ch1_pk (x output). P5.4 is the inhibit of IC28(U25).
- 3 - Delay 500 microseconds.
- 4 - Inputs of the peak hold circuits are set to 0 VDC by hooking them to DAC outputs and setting the DACs to zero volt. The DACs are set to 0 by writing 80H (zero decimal) to address FF40 and FF41 (refer to memory map). The next step is to modify port 5 to xxxxxx01. This points DAC1 to the x output of IC29(U29) which is the peak hold input. Finally port 5 is modified to xxx001xx. This directs the peak hold circuit output to the output of IC28(U25) which goes to the multiplexer IC17(U26) and finally to the ADC.
- 5 - Delay for 16 milliseconds for the peak hold circuit to stabilize.
- 6 - Read AD value. The AD value is read from analog board port 1. The HBD waits a maximum of 3.44 milliseconds for an interrupt from the AD converter (conversion successful). The interrupt comes in on bit 7 (1xxxxxxx) of analog board port zero. If the AD conversion was not successful (no interrupts in 3.44 ms wait period) a value of zero is used for comparison.

The value must be between 0.35 VDC and 1.0 VDC for test to pass.

5.4 Channel 1 Peak Hold Positive Test

There is a delay of 50 milliseconds between the execution of this sub-test and the previous test (zero test). This delay allows the capacitors to discharge completely. The peak hold positive test algorithm is the same as the peak hold zero test with the exception of the value written to DACs. In this test 2.8 VDC is written to the DACs (200 decimal to address FF40 and FF41). After the test is completed the ADC value must be between 2.396 VDC and 4.1 VDC for a successful test. Refer to section 5.3 (peak hold zero test) for more information on how the test is performed.

5.5 Channel 1 Peak Hold Capacitor Sag Test

The peak hold cap sag test algorithm is as follows:

- 1 - A positive voltage (2.8 VDC) is put into DACs by writing 200 to address FF40 (DAC1) and FF41 (DAC2).
- 2 - DACs are hooked to peak hold circuit by setting port 5 of the analog board to xxxxxx01. Bits p5.0 will point DAC1 to the input of peak hold while p5.1 enables the IC29(U29). Next port 5 is set to xxx001xx to connect output of peak hold circuit to ADC output of IC28(U25) actually goes through multiplexer IC17(U26) before reaching ADC).
- 3 - Wait until peak holds charge (16 seconds-second).
- 4 - Peak hold inputs are set to 0 VDC by hooking them to the DAC outputs and setting the DACs to 0 VDC. FF40 (DAC1) and FF41 (DAC2) receive 80H (zero). Port 5 of the analog board is then modified to xxxxxx01 which points DAC outputs to peak hold circuit IC29(U29).
- 5 - Wait 50 milliseconds.
- 6 - Read AD value. The AD value is read from analog board port 1. The HBD waits a maximum of 3.44 milliseconds for an interrupt from the AD converter (conversion successful). The interrupt comes in on bit 7 (1xxxxxxx) of the analog board port zero. If the AD conversion was not successful (no interrupts in 3.44 ms wait period) a value of zero is used for comparison.

If the peak hold capacitors do not retain their charge (at least 90 percent of the value written to them) the test fails. The peak hold capacitors must be between 2.318 VDC and 3.78 VDC.

5.6 Channel 2 Peak Hold Zero Test

Channel 2 Peak Hold Positive Test

Refer to section 5.3 (Channel 1 Peak Hold Test).

5.7 Channel 2 Peak Hold Capacitor Sag Test

Refer to section 5.4 (Channel 1 Peak Hold Cap Sag Test).

6 Second Level Test Error Messages

The following table lists all the error messages displayed **DATA DISPLAY** during the second level of board self test. If one of the following error messages is displayed (circuit has failed) the

HBD will repeat the same sub-test until the circuit passes the test or the DATA ADV switch is pressed to advance the board test to its next state.

DATA DISPLAY	Board Failure		Refer to
CPU CHIP	CPU	Micro-controller	1-11-21-3
CPU ROM0	CPU	EPROM0 checksum	1-4
CPU ROM1	CPU	EPROM1 checksum	1-4
CPU ROM2	CPU	EPROM2 checksum	1-4
CPU ROM3	CPU	EPROM3 checksum	1-4
RAM SEL	CPU	RAMs select lines	1-5
RAM ADDR	CPU	RAMs address lines	1-6
UPB RAM	CPU	RAMs internal structure	1-7
ROMx	(x is a digit)	Speech ROMs	2.0
IO PORT	Speech	Port 2	3.1
RST CAP	Speech	Port 2 Reset Caps.	3.2
PORT 0	Digital	Port 0	4.1
INTRRUPT	Digital	I/O Interrupts	4.2
PORT 1	Digital	Port 1	4.3
PORT 2	Digital	Port 2	4.4
RST CAP	Digital	Reset Capacitor	4.5
DAC 1	Analog	DAC 1 failed	5.1
DAC 2	Analog	DAC 2 failed	5.1
ADC	Analog	ADC failed	5.1
+5V	Analog	+5 VDC power source	5.2
-6V	Analog	-6 VDC power source	5.2
+12V	Analog	+12 VDC power source	5.2
-12V	Analog	-12 VDC power source	5.2
PKHLD1 O	Analog	Peak hold 1 zero test	5.3
PKHLD1 P	Analog	Peak hold 1 positive	5.4
CAP1 SAG	Analog	Peak hold 1 cap sag	5.5
PKHLD2 O	Analog	Peak hold 2 zero test	5.3
PKHLD2 P	Analog	Peak hold 2 positive	5.4
CAP2 SAG	Analog	Peak hold 2 cap sag	5.5

Setting/Display Alarm Parameters

Main Boards Utilized:

ANALOG BOARD, UNIVERSAL PROCESSOR BOARD

Theory Of Operation

There are six 10K pots on the analog board which are used to set/adjust the Hot Box Detector alarm parameters. Each 10K pot is used as a voltage divider tied between +5 volts and ground. These pots are 8 bits long (range from zero to 255). The Most Significant Bit(MSB) however, is used as the sign bit (same as all the hot box detector heat values). The remaining seven bits of magnitude produces a range of zero to 127 for negative values, and 128 to 255 for positive values (with a resolution of 39 mv per bit). This description uses millimeters as the unit of heat measurement.

The following parameters are assigned to each pot by the hot box detector software.

- * pot 1 (R28 on Analog II, R116A on Analog I)
Lo limit for simple (single) alarm analysis.
- * pot 2 (R29 on Analog II, R116B on Analog I)
Hi limit for absolute alarm analysis.
- * pot 3 (R30 on Analog II, R122C on Analog I)
Carside Slope for carside alarm analysis.
- * pot 4 (R31 on Analog II, R122D on Analog I)
Carside Lo limit for carside alarm analysis.
- * pot 5 (R32 on Analog II, R123E on Analog I)
Gate transducer spacing.
- * pot 6 (R33 on Analog II, R123F on Analog I)
Hot Wheel limit for hot wheel detector installations.

If The hot box detector software is not processing train data it reads and updates the pot values once every 50 milliseconds. This method keeps the pot values upto date while saving time during the processing of train data.

The hot box detector software stores the value of each pot in non-volatile memory on the serial I/O - time and date board. If the hot box detector software detects the presence of a time and date board, it will get the alarm parameters from the serial I/O - time and date board non-volatile memory, not the analog board voltage dividers (pots). Changing the pots on the analog board will not effect the values stored in the non-volatile memory. The only exception to this

rule is pot 5 (wheel gate spacing), which can be changed via analog board even if a time and date board is present. The only way the pot values can be set/adjusted when the time and date board is present is via DCP commands.

The DCP alarm mode offers several commands to set/adjust the pot values. These commands are normally used once during the initial installation. The hot box detector software retains the proper values after any power loss or system reset.

Adjusting the Analog Pots

This section describes how the pot values are read and adjusted by the hot box detector software. Note: this applies only if a DCP is not present.

The hot box detector software performs a checksum on the serial I/O - time and date board non-volatile memory values before each write, and after each read operation. This protect the hot box detector software against bad memory or a board malfunction. If the time and date board malfunctions the hot box detector software reverts to the analog board voltage dividers to get the required information. It is recommended to set the analog board pot settings to the correct values, even if a DCP board is installed at the site.

Each pot is an 8 bit value with the MSB used as the sign bit. The alarm parameters represented by the pots are all positive values with the possible range from 128 to 255 (128 being zero since the MSB is stripped off by the hot box detector software). The hot box detector software adjusts the physical value of each pot differently to scale it to the specific parameter. The hot box detector software has been programmed with a predefined minimum and maximum value for each parameter. The pot values are forced to these boundary values if the pot value is less than the minimum or greater than the maximum. Following are the current pre-defined values for the hot box detector software parameters:

Parameter		Minimum	Maximum
pot 1	Lo limit	5 mm	15 mm
pot 2	Hi limit	5 mm	24 mm
pot 3	Carside slop	0.68	2.36
pot 4	Carside Low limit	5 mm	15 mm
pot 5	Wheel Gate Width	15"	30"
pot 6	Hot Wheel limit		

Assigning Values to the Analog Pots

This section looks at the first pot reading as an example and shows how the physical value of the pot 1 voltage divider is adjusted by the hot box detector software to a logical reading used as the **Low Limit** alarm parameter.

The hot box detector software assigns 128 to the minimum output and 255 to the maximum output of the voltage divider. The MSB, which is one for positive values, is stripped off producing a range of 0 to 127. This is same as 0 to 25 millimeters with 5 units now equal one millimeter. This value is then scaled down by a factor of 2.5. The hot box detector software then adds 25 (5 millimeters - predefined minimum value for the Lo limit) to the pot value. This is the value saved for the Lo limit by the hot box detector software. The following two examples show how the minimum and maximum setting of the voltage divider (physical setting) is converted to the logical minimum and maximum parameter value.

Pot reading = 128 (minimum output of voltage divider):

step 1 - strip of the MSB : value = 0

step 2 - scale down by 2.5 : value = 0

step 3 - add 25 (5 mm) : value = 25 (5 mm)

Pot reading = 255 (maximum output of voltage divider):

step 1 - strip off MSB : value = 127

step 2 - scale down by 2.5 : value = 50

step 3 - add 25 (5 mm) : value = 75 (15 mm)

The following briefly describes the adjustments made to each pot.

pot 2 : scaled down by 2, add minimum 25

pot 3 : scaled down by 6, add minimum 68

pot 4 : scaled down by 5, add minimum 25

pot 5 : scaled up by 2, add minimum 15"

pot 6 : scaled down by 5, add minimum 25

First Pot:

The first pot is used to set/adjust the Low limit for the simple alarm analysis. The simple alarm analysis is performed on axles which have not been identified as a car. The following algorithm describes how the simple alarm analysis is performed and how the first pot value is used in the procedure.

For each out of sync axle (not recognized as a car) do

If (left side heat value > pot 1 value) then

 If (left side heat value > 3 * right side heat) then

 This axle has a differential alarm on left side.

If (right side heat value > pot 1 value) then

 if (right side heat value > 3 * left side heat) then

 This axle has a differential alarm on right side.

Second Pot:

The second pot is used to set/adjust the Hi limit for the absolute alarm analysis. The absolute alarm analysis is performed for every axle of the train regardless of the car recognition process. The following procedure describes how the value of the second pot is used during absolute alarm analysis.

For the current axle do

If (left side heat value > pot 2 value) then
This axle has an absolute alarm on left side.

If (right side heat value > pot 2 value) then
This axle has an absolute alarm on right side.

Third Pot:

Fourth Pot:

Third pot is used to set/adjust the Carside slope for the carside alarm analysis and the fourth pot sets/adjusts the Carside Low limit for carside alarm analysis. Carside analysis is performed on a group of axles (4 or 6 axles) which have been identified as a car/locomotive. The following algorithm describes how the hot box detector software performs carside alarm analysis and how the pot values are used in the algorithm.

a - Average heat is computed for the first side of the car.

a1 - Add all the heat values for side 1.

a2 - Subtract the largest and smallest heat values from the total heat.

a3 - Divide the result by (number of axles -2).

$$\text{average heat} = \frac{\text{total heat} - \text{largest heat} - \text{smallest heat}}{\text{number of axles} - 2}$$

b - Compute the carside alarm level for this car using the following formula:

$$\text{Alarm level} = \text{CS slope} * \text{average heat} + \text{CS limit} - \text{CS slope.}$$

Where: CS slope is pot 3.
CS limit is pot 4.

c - Compare the heat value (side 1) for each axle in this car against the computed Alarm level. If any axle heat is greater than the computed Alarm level, there is the possibility of an alarm.

d - If the side 1 heat value is greater than the Alarm level, the following alarm validation test is performed:

If the heat value of side 2 (non-alarm side) is less than 50% of the heat value of side 1 (possible alarm side) then a CS alarm is present. Note: 50% is a predefined software constant. To change this value contact Harmon Electronics, Inc.

The above procedure is repeated for the same car using the side 2 heat values.

Fifth Pot:

The fifth pot is used to set/adjust the gate transducer spacing. The gate transducer spacing is stored in inches and can range from 15" to 30". The fifth pot value plays an important part in the following functions:

- * Train speed.
- * Train length.
- * Car recognition procedure.
- * Carside alarm analysis.

The time interval taken for each axle to travel from gate A to gate B transducer is calculated by the hot box detector software. Using this time interval and the pot 5 value, the hot box detector software calculates the axle speed. Other functions of the hot box detector software use the train speed and pot 5 value to perform their tasks.

Software Interface

The function that reads the pot values is called once every 50 milliseconds. This section describes the steps taken to perform this task.

perform the following for each pot:

1. Disable the interrupts.
2. Send the address of the pot and the access code to the 16/1 analog multiplexer.
3. Start the A to D conversion.
4. Wait a maximum of 3.44 milliseconds or until the A to D conversion is complete.
5. Enable the interrupts.
6. If the A to D conversion was complete then read the value from the A to D buffer.
otherwise read zero for the value indicating an error.
7. Perform the specific scaling for the current pot.
8. Save the pot value.

Hardware Interface

The following algorithm describes how the pots are read by the hardware.

1. Disable interrupts.
2. Write the pot address and access code to the A to D controller (A to D controller is at analog+6, access code is).

3. Start A to D conversion.
 - 3a. - Send start A to D conversion mask to the A to D controller (20H).
 - 3b. - Send stop A to D conversion mask to the A to D controller (DFH).
 - 3c. - Enable the interrupts.
4. Read the value of the A to D conversion buffer.
 - 4a. - Wait a maximum of 3.44 milliseconds or until interrupted by the A to D conversion (get ADC ready, which is 80H, from analog interrupts, which is at analog+0).
 - 4b. - If the A to D conversion was complete (interrupted) read the A to D data, otherwise read zero indicating an error (A to D data is at analog +01).

The address for each pot is as follows:

Pot	Address
1	15 Hex
2	0D
3	16
4	0E
5	14
6	0C
7	15 (second Analog Board)

Display Pots

If the hot box detector front panel **MODE** switch is placed in position 'A' and the hot box detector is not processing a train, the **DISPLAY POTS** function is activated. Following is an description of what each of front panel switch is used for during the display pots function.

The **FUNCTION** switch determines the format the hot box detector software uses to display the pot value. If the **FUNCTION** switch is set to position 1 the hot box detector software displays the actual reading from the A/D converter in the **DATA DISPLAY**. This value ranges from 128 to 255. As described previously, the hot box detector software scales this value depending on the function of the parameter. If a time and date board is present the **DATA DISPLAY** will show 'DCP ON' instead of the pot value. This is done to notify the user that the hot box detector software uses its non-volatile memory to read the pot settings not the analog board pots. If the **FUNCTION** switch is in the middle the **DATA DISPLAY** shows the name of parameter which corresponds to the current pot. If the **FUNCTION** switch is in position 2 the **DATA DISPLAY** shows the modified value of the pot. The value for pot 1, pot 2, and pot 5 are displayed in millimeters, the value for pot 3 is displayed in decimal, and pot 5 is displayed in inches. These are the actual values used by the hot box detector software during the processing of train data.

The **DATA ADVANCE** switch is used to display the next available pot. When the **DATA ADVANCE** switch is pressed the **DATA DISPLAY** will change to show the value/name of the next pot.

The **RESET** switch will instruct the hot box detector software to go back to the first pot and display it.

Display the Actual Pot Value

If the **FUNCTION** switch is set to position 1, the **DATA DISPLAY** will show the reading from the pot voltage divider. If a DCP is present the hot **DATA DISPLAY** shows the phrase 'DCP ON'.

If the hot box detector is configured as a hot wheel detector(12 possible pots), the **DATA DISPLAY** shows:

$R A_x = yyy$
where x can be 1, 2, 3, 4, 5, or 6.
 yyy is the pot reading.
 A indicates the pot values from first analog board.

When the **DATA ADVANCE** switch is pressed the pot number is incremented to a maximum of 6, when the display changes to

$R B_x = yyy$
where x is the pot number (1 to 6)
 yyy is the pot reading.
 B indicates the pots values of second analog board.

As the **DATA ADVANCE** switch is pressed the pot number is incremented to a maximum of 6. The **DATA DISPLAY** displays the first analog board pots. If the hot box detector software is not configured as a hot wheel detector (6 possible pots) the **DATA DISPLAY** shows:

$R_x = yyy$
where x is the pot number (1 to 6).
 yyy is the pot value.

As the **DATA ADVANCE** switch is pressed the pot number is incremented to a maximum of 6. The **DATA DISPLAY** then displays the first pot again.

Display Parameter Names

If the **FUNCTION** switch is in the middle the **DATA DISPLAY** shows the parameter name which is assigned to the current pot. One of the followings will be displayed:

LO LIMIT	Simple(single) lo limit
HI LIMIT	Absolute hi limit
CS SLOPE	Carside slope
CS LIMIT	Carside lo limit
WHL GATE	Gate transducer spacing.
NOT USED	
HW LIMIT	If second analog board is present, HW limit.

Recorder Calibration Mode

Theory of Operation

"Recorder Calibration" mode, position 'D' on the **MODE** switch, allows service personnel to insure that the analog chart recorder is correctly aligned. Reference peaks are generated to allow for precise calibration. Calibration is very important since heat values obtained from a real train are written to the chart recorder to give a visual indication of the amount of heat seen trackside. If the calibration is inaccurate the actual heat readings may also be appear to be inaccurate when they are actually very precise. Heat pulses are printed on the chart paper and should be aligned with the pre-printed lines on the chart paper.

This description will only cover the software operation of the "Recorder Calibration" and will not cover the actual calibration procedure if required. This can be found in the Model 27 Recorder manual.

"Recorder Calibration" mode is entered by placing the **MODE** switch in the position 'D'. The **DATA DISPLAY** will give the message "RCDR CAL". Pressing the **DATA ADV** switch initiates a series of 5, 10, 15, and 20 millimeter high pulses on the analog chart recorder. The pulses are printed on both channel one and channel two. "Recorder Calibration" can be reset by pressing the **RESET** switch, moving the **MODE** switch to another position, or the approach of a train.

Software Interface

The "Recorder Calibration" software is written in two states of actual operation. One state prints a pulse for twenty milliseconds and the other state waits for one hundred milliseconds. When the **MODE** switch is placed in position 'D' the **DATA ADV** is monitored for activity. If the **DATA ADV** switch is pressed the "Recorder Calibration" software begins writing pulses to the chart recorder.

As stated above, pulses are written to the chart recorder for twenty milliseconds. Each pulse is twenty milliseconds wide and five millimeters higher than the one in front of it. After each pulse is written to the chart recorder a zero millimeter pulse is written for one hundred milliseconds. This is done to show some separation and allow time to make adjustments as required.

The initial pulse is zero millimeters in height. Each pulse written after that is incremented by five millimeters until the pulse reaches twenty millimeters. The next pulse after the twenty millimeter pulse will again be zero. The pulses appear as a ramp of pulses and are repeated until the "Recorder Calibration mode is halted. The pulses that are written to the chart recorder are the same as the pulses that are written after every tenth train.

If it is necessary to adjust the chart recorder refer to the Model 27 Chart Recorder manual for the adjustment procedure.

Tone Test/Temperature Display Mode

Ambient Temperature Display

The "Tone Test" and "Temperature Display" modes are entered by placing the **MODE** switch in position 'F'. The specific mode is dependent upon the position of the **FUNCTION** switch. Placing the **FUNCTION** switch in position '1' (left position) will display the ambient temperature on the **DATA DISPLAY**. The display can be toggled between the internal and external ambient temperatures by pressing the **DATA ADV** switch.

The external ambient temperature monitor is controlled by front panel DIP switches and the internal ambient temperature is controlled by DIP switches located on the Universal Processor Board. Refer to the software documentation for specific location and function of the DIP switches and ambient temperature reporting functions.

The external ambient temperature monitor is connected to the analog board channel 3 and the internal ambient temperature is connected to the analog board channel 6. The ambient temperature inputs interface to the analog board through the ambient temperature input network IN3. The ambient temperature is updated every 50 milliseconds and is used in several functions in the HBD software. To update the ambient, external or internal, the software writes the address of the channel to be sampled the AD convertor. The same the time that the channel is selected to be converted a bit is also included that starts the AD conversion.

The first 3 bits of the bit pattern that is written to the multiplexer, IC17(U26) or IC20(U27) determines which channel is going to be converted. Bits 3 and 4 determine which multiplexer is enabled and which multiplexer is disabled. When bit 5 is toggled the A to D conversion is started. The output of the multiplexer is then directed to the ADC IC19(U21). The data read off of the ADC is then converted into a temperature value.

The conversion routine returns a voltage level that is then converted into a positive or negative temperature. The range of the temperature is between -55°C (-67° F) and 71°C (128°F). The conversion process is performed as follows:

1. 0 VDC = -55° C or -67° F
2. If the ambient temperature is less than -55° C.
Then the ambient temperature = -55° C.
Else the ambient temperature = the ambient temperature - 55° C.
3. Negative temperature flag = 0. The temperature is non-negative. The negative temperature flag is used to flag negative temperatures.
4. If the ambient temperature is < 128 then the ambient temperature = 128 - ambient temperature and the negative flag = 1. The ambient temperature is now negative.
Else the ambient temperature = ambient temperature - 128.
5. The temperature is converted from degrees Celsius to degrees Fahrenheit.

This procedure is performed for both the internal ambient temperature and the external ambient temperature. The results are printed on the chart recorder, transmitted to the DCP, and spoken at the end of train passage.

Tone Test

A test tone is available to be used in adjusting the local radio transmit levels and the local speaker volume. To initiate a test tone place the **MODE** switch in position 'F'. The **FUNCTION** switch must be placed in the center position. The **DATA DISPLAY** will show the phrase "TONE TST". When the **DATA ADV** switch is pressed a continuous 1000Hz tone is transmitted over the local radio and local speaker. The 1000 Hz tone is constantly transmitted until the system is reset by the approach of a real train or by pressing the **RESET** switch.

Time and Date Routine

Theory Of Operation

The MC146818 Real Time Clock (RTC) plus RAM is used for

- ◆ Time of day clock
- ◆ 100 year calendar
- ◆ Fifty (50) bytes of static Non-Volatile RAM.

The usage of MC146818 RTC (U5) is twofold. First, the RTC relieves the HBD software of the timekeeping workload and it can be used as an extended Non Volatile RAM. The time and date board provides 128 bytes of Non-Volatile RAM (U3, U4, U8, U9 are 4x256 memories that act together to make up 128 bytes). However, the RTC extended RAM are not currently used by the HBD software.

The MC146818 RTC has other functions that are not currently used by the HBD software; i.e, RTC interrupt features.

The MC146818 RTC provides the time and date data for both HBD, and DCP. The RTC becomes a part of the HBD memory map. Therefore, the HBD directly controls the RTC, while the DCP can access the RTC indirectly via connector J2. The communication between DCP and RTC is through serial channel JA into U14 (U16 and U17 together make up JA). U14 in turn converts the DCP serial data into a parallel format for the RTC. U14 also converts the RTC parallel data in serial format to transfer to the DCP. Refer to DCP document for more information on how/when the DCP accesses the RTC).

It is very important to note that the HBD transmits the current time and date as part of the train data to the DCP. When DCP receives the time and date information from HBD (End Of Train data). The DCP will then reset its time and date buffer to the data transmitted by the HBD.

The MC146818 RTC provides a 100 year calendar, from 1983 to 2083.

The RTC is driven by a 32.768 KHz crystal oscillator (Y2 across pin 2 and 3 of RTC). The HBD DATA DISPLAY gives the message "OBSOLETE" if the calendar is out of the 100 year range.

Other features of the MC146818 RTC are "automatic end of month recognition", and "automatic leap year compensation". Therefore, the HBD software does not examine the RTC time and date data for its validity.

The MC146818 RTC contains 64 bytes of memory. Figure 1 demonstrates the memory map of RTC. Ten (10) bytes of the memory are used by the RTC to store the current time and date data. As seen, 4 bytes of the data are not used by the HBD. The other six bytes are read once every 50 milliseconds to update the HBD time and date buffer. These 6 bytes are also modified by HBD, when the user wishes to set/adjust the current time and date.

The next four (4) bytes are used to control the RTC, or examine the status of RTC before modifying its internal data.

Bytes 14 to 63 are available to the HBD 8031 micro-controller as an extended RAM. Currently, HBD software does not utilize the memory space.

Byte	Function	Comments
0	Seconds	Read/written by the HBD
1	Seconds Alarm	Not Used
2	Minutes	Read/written by the HBD
3	Minutes Alarm	Not Used
4	Hours	Read/written by the HBD
5	Hours Alarm	Not Used
6	Day Of Week	Not Used
7	Date Of Month	Read/written by the HBD
8	Month	Read/written by the HBD
9	Year	Read/written by the HBD
10	Register A	RTC Control/Status Reg.
11	Register B	RTC Control/Status Reg.
12	Register C	RTC Control/Status Reg.
13	Register D	RTC Control/Status Reg.
14	Available RAM	Not Used
..	..	..
63	Available RAM	Not Used

Figure 1. Memory map of the RTC

RTC Register A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIP	DIV2	DIV1	DIV0	RS3	RS2	RS1	RS0

Bit 7 (Update In Progress) signifies if the RTC is in transition. The RTC data is read/modified if the UIP bit is at zero.

Bits 6, 5, and 4 select one of the RTC 22-stage divider. The HBD software set these bits to (010) to select the 32.768 KHz time base.

Bits 3, 2, 1, and 0 are the rate selectors. The HBD sets these bits to (0011) to set the RTC periodic interrupt rate at 122.070 micro-seconds.

RTC Register B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

The HBD software controls the RTC via bit 7. Setting Bit 7 to zero, disables the RTC update functions. Therefore, the HBD software can modify the content of RTC time/date data.

Bit 2 of register B (Data Format) selects one of the binary or Binary Coded Decimal (BCD) format. The HBD sets bit 2 to 1, instructing the RTC to use the binary format.

Bit 1 signifies the format of hour. The HBD uses the 24-hour format, thus setting bit 1 to 1.

Bit 0 (Daylight Saving Enable), bit 3 (Square Wave Enable), bit 4 (Update ended Interrupt Enable), bit 5 (Alarm Enable Interrupt), and bit 6 (Periodic Interrupt Enable) are not used by the HBD software.

RTC Register C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF	PF	AF	UF	NU	NU	NU	NU

The RTC register C is not used by the HBD software. They are IRQF (Interrupt ReQest Flag), PF (Periodic interrupt Flag), AF (Alarm interrupt Flag), UF (Update ended interrupt Flag). Bits 0, 1, 2, and 3 are not used by the RTC.

RTC Register D

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRT	NU	NU	NU	NU	NU	NU	NU

Bit 7 (Valid RAM and Time) indicates the condition of the contents of the RTC RAM.

Bits 0 to 6 are not used by the RTC.

Power Up RTC Initialization

On power up, the HBD software looks for the presence of the time and date board. Presence of RTC can be determined by writing a specific value to one of the 50 bytes RAM space of the RTC. The RAM location can be examined after a short delay, to determine if a RTC is present.

At this point, an internal flag is set/reset signifying the presence/absent of RTC to other HBD functions which use the RTC. If the presence of RTC is detected, the following operations are performed to initialize the current time and date:

Initially RTC register A is examined for proper Rate Selector. Bits zero, 1, 2, and 3 of register A must be set to xxxx0011 to force the 122.070 micro-second interrupt rate.

At this point, bit 7 of RTC register A (Update In Progress) is examined. If the RTC is not in transition, the current time and date of RTC is read and stored in the time/date buffer.

The final step during power up RTC initialization is to examine the content of RTC RAM for their validity. Bit 7 of RTC register D(Valid RAM and Time) indicates the condition of RTC data. set to If the RTC data is not valid (bit 7 is zero), the Power Loss Initialization is performed.

Power Loss Initialization

The Power Loss Initialization is performed if bit 7 of RTC register D (VRT) is zero, indicating invalid RTC RAM data. Bit 7 is negated when pin 22 of RTC (Power Sense) goes low.

The Power Loss initialization routine sets the RTC register A to 0010,0011 (time base frequency of 32.768 K Hz, and 122.070 micro-second interrupt rate), and RTC register B to 1000,0110 (allow data update, force binary format, and use 24-hour format).

Finally the time and date bytes are reset to their minimum values. The year is set to 1985, while month, day, hour, minute, and second are set to one (1).

Modifying Time/Date Via DCP Commands

DCP maintenance mode commands assist the user to set/adjust the current time and date of the Hot Box Detector.

It is very important to note that the HBD does not accept the time and date command (from DCP) if a train is passing the detector. The only time when HBD services the DCP command is when the HBD is in its ideal state (No Train Around).

The first step is to check the validity of user input.

- ◆ The year must be greater than 1983, and less than 2084.
- ◆ The month must by greater than zero and less than 13.
- ◆ The day must be grater than zero and less than 32.
- ◆ The hour must be less than 24.
- ◆ The minute must be less than 60.
- ◆ The second must be less than 60.
- ◆ If the month is 4, 6, 9, or 11 (Apr, Jun, Sep, Nov), the day must be less than 31.
- ◆ For a leap year, and second month (Feb), the days must be less than 29.

In case of improper user input, the HBD simply ignores the time and date command from DCP.

However, if the user input is valid, the RTC register A is examined for transition state of RTC. As soon as the RTC sets the bit 7 (UIP) to zero (Not In Transition), the new time and date is written to the RTC.

The same values written to the RTC are also written to the HBD time and date buffer.

Modifying Time/Date Via HBD Front Panel Switches

The user can view or set/adjust the HBD current time and date, by setting the **MODE** switch to position 'C'.

The user can select the function of time and date routine by using the **FUNCTION** switch. If the **FUNCTION** switch is placed to the middle position the time and date routine will be in its display mode. Setting the **FUNCTION** switch to position '1' or position '2' places the time and date routine in the update mode.

Display Mode

The "Display" mode of time and date routine displays the current time and date every 50 milliseconds. During the "Display" mode, the only front panel switch used is the **DATA ADV** switch.

Initially the current year is displayed. The user can press **DATA ADV** switch to view the next time and date field, i.e. current month, day, hour, minute, and seconds.

Following are examples of the displayed data:

- ◆ YR: 1992
- ◆ MONTH= 9
- ◆ DATE= 30
- ◆ HOUR= 14
- ◆ MINS= 25
- ◆ SECS= 35

Update Mode

The user can instruct the HBD to set/adjust the current time and date by setting the **FUNCTION** switch to the position '1' or position '2'. In the "Update" mode, two switches are used. The **DATA ADV** switch is used to select the time and date field that needs to be adjusted. The **FUNCTION** switch is used to increment or decrement the displayed field.

By pressing the **DATA ADV** switch, the user can select the particular field that needs to be adjusted. At this point, the user can press the **FUNCTION** switch to position '1' to decrement

the displayed field. The displayed field can be incremented, if the **FUNCTION** key is placed in position '2'.

Initially the time and date routine will display the current field. If the **FUNCTION** switch is set to position '2', the field is incremented two times a second. However, if the **FUNCTION** switch is set to position '1', the field is decremented two times a second.

The next step is to examine the new value for the displayed field. For example, if the month is within 1 and 12, its value is accepted. However, if month is 13, it is set to one 1 (increment mode). If the month is zero, it is set to 12 (decrement mode).

Next step is to examine the new value of the current field with other fields of time and date data. For example, the days is adjusted if the current year is a leap year, and the month is Feb.

At this point, RTC register A is examined for RTC transition state. If RTC is not in the transition, the new time and date data is written to the RTC.

The same time and date data is stored in the HBD time and date buffer, and displayed to the front panel display.

The operations described above are repeated until the **MODE** switch is changed or the **FUNCTION** switch is placed in the middle position.

Port Data Display

Main Boards Utilized

DIGITAL AND SPEECH BOARD

Theory of Operation

With the **MODE** set to the **PORT DATA DISPLAY** position the HBD sends the data present on the digital ports to the front panel LEDs. The front panel has 8 vertically positioned LEDs which represent the 8 bits of a particular port. In the **PORT DATA DISPLAY** mode, the markings to the left of the LEDs, which mark the top LED as bit 0 and the bottom LED as the bit 7, should be used. An LED will be on if the corresponding bit is grounded (active), and off if a potential of 12 VDC exists across the input. This is one of the methods available to assist in troubleshooting the HBD digital ports. This function can also be used to detect any stuck inputs.

Operation

The HBD displays the port number (0 to 255) in hexadecimal format. A two digit hex value is used to represent the port number.

The port number to be is displayed on the **DATA DISPLAY** and can be incremented or decremented using the front panel switches. The **FUNCTION** switch determines how the HBD increments or decrements the port number when the **DATA ADV** switch is pushed. If the **FUNCTION** switch is set to position '1', the HBD increments the left digit of the port number. If the **FUNCTION** switch is set to position '2', the HBD increments the right digit of the port number. If the **FUNCTION** switch is set in the normal (center) position, the HBD decrements the port number by one.

Software Interface

If the **MODE** switch is set to the **PORT DATA DISPLAY** position, the HBD invokes the "display port" function. This section lists the steps taken by this function to display the port values.

The port number initially has a value of zero after power-up or system reset. When the 'display port' function is called, it reads in the current status of the port identified by the port number. The function then updates the front panel LEDs according to the port value. The 'display port' function then monitors the front panel switches. Upon activating any of the switches as previously described, the function takes the proper steps to perform the user request. The following shows how the 'display port' function performs its task:

- While the **MODE** switch is set to the **PORT DATA DISPLAY** position, perform the following steps:
 - If the **DATA ADV** switch is pressed do one of the following:

- If the **FUNCTION** switch is set to position '1' then add 16 to the port number.
- If the **FUNCTION** switch is set to position 2 then add one to the port number.
- If the **FUNCTION** switch is set to the normal (center) position then subtract one from the port number.
- Read in and invert the port value.
- Update the front panel LEDs.

Since the HBD hardware uses negative logic (ground is logic one), the value read in from the digital ports (step 6) must be inverted before it is displayed on the front panel LEDs (step 7).

BIT Map of Digital Ports

In current HBD systems the digital board uses three digital ports, and the speech board uses one digital port. The address for each port is given below. While any address may be displayed, the following are the only addresses that will produce useful data.

Board	Port #	Address
Dig.	0	00 Hex
Dig.	1	01 Hex
Dig	2	02 Hex
Speech	0	82 Hex

Digital Board Port 0

Bit	function	HBD back panel	Dir
0	Aux 1, Ch1 Hot Box	TB10-1	O
1	Aux 2, Ch2 Hot Box	TB10-2	O
2	Aux 3, Dragging Equip	TB10-3	I
3	Aux 4, High Load	TB10-4	I
4	Aux 5, Wide Load 1	TB10-5	I
5	Aux 6, Wide Load 2	TB10-6	I
6	Aux 7, Not Used	TB10-7	--
7	Aux 8, Wheel Gate	TB10-8	O

Digital Board Port 1

Bit	function	HBD back panel	Dir
0	Direction 1 input	TB12-1	O
1	Direction 2 input	TB12-2	O
2	Track Circuit	TB12-3	I
3	Aux Recorder Drive	TB12-4	O
4	Event Pen Drive	TB12-5	O
5	System Integ Drive	TB12-6	O
6	Main Alarm Drive	TB12-7	O
7	Ext Power Status	TB12-8	I

Digital Board Port 2

Bit	function	HBD back panel	Dir
0	Not Used	TB14-8	--
1	Integ Test Lamp Drive	TB14-9	O
2	Prot Shutter Drive	TB14-10	O
3	Prot Shutter Switch 1	TB14-11	I
4	Prot Shutter Switch 2	TB14-12	I
5	Real Train Passing	TB15-1	O
6	Open Optical Shutter	TB15-2	O
7	Close Optical Shutter	TB15-3	O

Speech Board Port 0

Bit	function	HBD back panel	Dir
0	Transmitter On/Off Control		--
1	RF Detect/Tunnel Circuit		O
2	Radio Transmit Off		I
3	HBD Disable		I
4	Prot Shutter 3 Switch		O
5	Prot Shutter 4 Switch		O
6	Transmitter Request		O
7	Other HBD Trans. Request		I

For more information regarding individual bits, refer to the digital I/O section of this manual. The following information is available for the individual bits:

- When the HBD software reads in each bit.
- How the HBD uses each bit in its process train cycle.
- How the output bits are used.
- Ideal and active state of each bit.

Digital and Speech I/O ports

Main Board Utilized

DIGITAL AND SPEECH BOARDS

Theory of Operation

The digital input/output (I/O) board consists of three general purpose 8 bit ports, while the speech board has one 8 bit port. This section describes what each, bit encoded, port is used for.

Digital Board - Port 0

Port 0 (at address FF00 hex) is used for auxiliary alarm inputs, and the wheel gate flag. The bits are encoded as follow:

Bit	function	HBD back panel	Dir
0	Not Used	TB10-1	--
1	Not Used	TB10-2	--
2	Aux 1, Dragging Equip.	TB10-3	In
3	Aux 2, High Load	TB10-4	In
4	Aux 3, Wide Load 1	TB10-5	In
5	Aux 4, Wide Load 2	TB10-6	In
6	Not Used	TB10-7	--
7	Wheel gate intr.	TB10-8	Out

Bit 0 and 1 of port 0 is not currently used. These two bits were used as an event pen driver for the chart recorder by older versions of software. Therefore a potential of 12 VDC exist across these inputs at all times.

Bit 2, 3, 4, and 5 are used for auxiliary alarm inputs. These inputs are controlled by the trackside equipment. To inform the HBD of the presence of an alarm, the trackside equipment grounds the specific bit. The HBD reads the alarm inputs after the axle has crossed the gating transducer (refer to transducer interrupts for timing detail of this operation). During the functional self test, several auxiliary alarms are simulated using the bidirectional latch for the port 0.

The AUX alarm inputs are examined once every two minutes (two minute integrity test). The HBD reports an integrity failure if any of these inputs are stuck opened (grounded).

Bit 7 of port 0 is used by the HBD to inform the arrival and the departure of an axle. As described "Transducer Inputs" section of this document each axle generates 4 interrupts. The HBD grounds TB10-8 output at interrupt point 1 (arrival of axle), and disables the output (12 VDC) at interrupt point 4 (departure of axle).

The front panel "WHL GATE" LED uses this input to operate during train passage. The

"WHL GATE" LED will turn on if the bit is set, and remains off otherwise.

Digital Board - Port 1

Bit	function	HBD back panel	Dir
0	Direction 1	TB12-1	Out
1	Direction 2	TB12-2	Out
2	Track Circuit	TB12-3	In
3	Aux Recorder Drive	TB12-4	Out
4	Recorder Event Pen Drive	TB12-5	Out
5	System Integ Drive	TB12-6	Out
6	Main Alarm Drive	TB12-7	Out
7	Not Used	TB12-8	--

BIT 0, 1: TRAIN DIRECTION

Bit 0 and 1 of port 1 are used to indicate train direction. Since the HBD front panel DIP switches determine train direction, and format of speech annunciation, the direction is referred to directions 1 and 2.

During the no train around state both outputs should be high (12 VDC).

The HBD function which processes transducer interrupts updates bit 0, and 1 accordingly. Train direction is determined by the sequence of interrupts received from the gating transducers. Bit 0 and 1 are also used by other HBD functions to perform their tasks. During train passage one of the outputs should be grounded indicating train direction. If both outputs are grounded simultaneously an error has occurred. In this case an error message will be sent to DCP, and chart recorder.

BIT 2: TRACK CIRCUIT INPUT

Upon arrival of a train, the HBD needs to be informed so that it can perform its pre-train functions. This includes the pre-train integrity test. The track circuit input is used as a wake-up signal. Upon receiving the signal from the track circuit (bit 2 is grounded), the HBD disables any front panel functions which are being executed (board self test, test train,...). It also opens the scanner protective shutters, and performs the scanner integrity test (along with the system integrity test).

If the HBD is instructed to simulate a test train, it will use this input to simulate train arrival. Bit 2 should be at 12 VDC during HBD standby.

BIT 3: CHART RECORDER DRIVE

Bit 3 of port 1 controls the chart recorder. The HBD grounds this bit to turn the recorder on. HBD turns the recorder on during

- * Real train passage.
- * Test train simulation.
- * Chop function.
- * Recorder Calibration.

Once every 50 milliseconds, the HBD updates bit 3 status. If one of the above functions is being executed, HBD will ground the output, otherwise it will force a potential of 12 VDC across the output.

BIT 4: CHART RECORDER EVENT PEN DRIVE

This bit should be high at idle state (no train around). This output will be grounded if HBD detects any alarms. In this case HBD will ground the output for a period of 10 milliseconds, after which it will disable it again (12 VDC). Grounding the event pen output generates a vertical blip on the chart recorder. Please note that the output is grounded regardless of alarm type.

BIT 5: SYSTEM INTEGRITY DRIVE

This output is also updated once every 50 milliseconds. Bit 5 controls the status of the integrity lamp. If system integrity is good, the output will be on (grounded), and off to indicate bad integrity (12 VDC). As mentioned perilously, the HBD performs a system integrity test once every two minutes. This output will then indicate the status of the test.

BIT 6: MAIN ALARM DRIVE

Bit 6 of port 1 performs the same function as bit 4 of port 1, with the exception that once grounded, it will remain grounded until end of train timeout.

During train passage (also test trains), as soon as an alarm is detected (regardless of alarm type), bit 6 will be grounded to indicate train has an alarm. The status of bit 6 remains unchanged until HBD finishes its end of train operations (speech annunciation, and chart recorder output).

DIGITAL BOARD PORT 2

Bit	function	HBD back panel	Dir
0	Not Used	TB14-8	--
1	Integ Test Lamp Drive	TB14-9	Out
2	Prot Shutter Drive	TB14-10	Out
3	Prot Shutter Switch 1	TB14-11	In
4	Prot Shutter Switch 2	TB14-12	In
5	Real Train Passing	TB15-1	Out
6	Open Optical Shutter	TB15-2	Out
7	Close Optical Shutter	TB15-3	Out

BIT 1: INTEGRITY TEST LAMP DRIVE

Upon arrival of a train, HBD performs a pre-train integrity test which includes testing the scanner circuits. After opening the protective shutters, HBD will turn on the lamp inside the scanners. At this point HBD reads in the heat generated by the lamp, and compares it against a pre-defined value.

Thus bit 1 of port 2, is always at 12 VDC potential, except during train arrival which will momentary will be grounded to turn the lamp inside scanners on for a few moments.

BIT 2: PROTECTIVE SHUTTER DRIVE

This output controls the scanner protective shutter mechanism. It should be at 12 VDC if no train is passing the detector. HBD will ground this output (open the protective shutters) upon train arrival, and keeps it at ground potential until end of train timeout. HBD will close the protective shutters (output at 12 VDC) before it performs its end of train operations (announcements, char recorder,...).

BIT 3, AND 4: PROTECTIVE SHUTTER SWITCHES

The scanner solenoid switches control these two inputs. They are at ground potential if the protective shutters are open, and at 12 VDC if they are closed.

During pre train integrity test, HBD checks the status of protective shutters. At first HBD expects a high voltage across both inputs (shutters are closed). HBD will then open the shutters, and re-examine the status of the inputs. At this time both inputs must be at ground potential (shutters are open). In case of any failure, HBD will announce bad integrity message, transmit proper message to DCP, and writes the fault to the chart recorder.

BIT 5: REAL TRAIN PASSING

This output should be at 12 VDC unless a real train is passing the detector. The output is updated once every 2.5 milliseconds. If a real train is passing, HBD grounds the output, otherwise HBD will set the output at 12 VDC.

BIT 6, AND 7: OPTICAL SHUTTER DRIVE

These outputs are used to open/close the scanner optical shutters. When HBD receives an interrupt from first gating transducer (axle arrival), the optical shutters are opened. The optical shutters are then closed when the axle leaves the second gating transducer. Refer to the "Wheel Transducer" section for more information on timing and interrupt points. Once the optical shutters are closed, the scanner compares the heat value (when shutters were open) to the scanner inside temperature.

Speech Board I/O Port

The speech board includes 8 general purpose I/O circuits. In this section of document, functions of each I/O circuit is described.

Bit	Function	HBD back panel	Dir
0	Transmitter on/off control	TB9.1	Out
1	Tunnel Circuit	TB9.2	In
2	Radio Mute	TB9.3	Out
3	HBD Disable	TB9.4	Out
4	Protective shutter 3 switch	TB9.5	In
5	Protective shutter 4 switch	TB9.6	In
6	Transmitter request	TB9.7	Out
7	Other HBD transmitter Request	TB9.8	In

BIT 0: TRANSMITTER ON/OFF CONTROL

This is the output which keys the radio on. Once every 50 milliseconds HBD updates the output status. If any of the HBD tasks require the radio, HBD grounds the bit to key the radio on. Currently only two tasks have access to the radio, real train announcements, and tone test (front panel position "F"). Please note that the radio will not be keyed on if HBD radio is mute (for more information refer to Radio Mute/Unmute).

BIT 1: TUNNEL CIRCUIT

The tunnel circuit input provides a means to have the last end-of-train message re-broadcast to the train crew. The tunnel circuit, as the name implies, is a track circuit device that is typically placed on the other side of a tunnel so that the end-of-train message can be re-broadcast to the train crew when it could be highly probable that the train was in the tunnel when the message was broadcast the first time.

This input acts the same as a "DATA RECALL" replay does. It broadcast the last end-of-train message one time after the input has been activated. It can be reset if a new train comes into the HBD area or if the **RESET** switch is pressed.

BIT 2: RADIO MUTE/UNMUTE

One of the new features of HBD is the ability to mute the radio (for more information refer to Radio Mute/Unmute). This output indicates the status of radio. If radio mute is enable (HBD does not key the radio on), this output will be grounded, otherwise it will be at a potential of 12 VDC.

BIT 3: HBD DISABLE/ENABLED

One of the new features of HBD is to prevent the HBD from processing train data (for more information refer to HBD Disable). This output shows current status of HBD disable feature. If HBD has been disabled, the output will be at zero potential.

BIT 4, AND 5: PROTECTIVE SHUTTER SWITCHES

These two outputs are only used if the system has been configured as a Hot Wheel Detector. In this case the second set of scanners (Hot Wheels) control these inputs. During pre train integrity test, HBD checks the status of protective shutters. At first HBD expects a high voltage across both inputs (shutters are closed). HBD will then open the shutters, and re-examine the status of the inputs. At this time both inputs must be at ground potential (shutters are open). In case of any failure, HBD will announce bad integrity message, transmit proper message to DCP, and writes the fault to the chart recorder.

BIT 6: TRANSMITTER REQUEST

BIT 7: OTHER HBD TRANSMITTER REQUEST

Two HBDs can be connected to use the same radio. These two bits manage the use of radio between the two HBDs. Bit 6 (xmitter request) is an output, which is grounded whenever the HBD is using the radio. Bit 7 on the other hand, is an input, which informs the HBD if another HBD is using the radio.

Before using the radio, HBD checks the status of bit 7, if the input is at 12 VDC (no one is using the radio), it will transmit its messages right away. However, if the input is at ground potential (another HBD is using the radio), it will wait a maximum of 5 minutes. After the 5 minute wait period, HBD will transmit its messages regardless of status of the input (it will also set a flag for DCP, and chart recorder).



Scanner Heat

Main Boards Used

ANALOG BOARD, UNIVERSAL PROCESSOR BOARD, DIGITAL BOARD, OVERLAY BOARD

Theory of Operation

The scanner compares infrared energy emitted from the bearing to the radiation of the built-in reference shutter. The reference shutter temperature is near ambient. A germanium lens permits the infrared (8-14 μ m) or heat energy to pass to the detector, while avoiding interference from reflected light.

The scanner does not use the principle of a thermometer; it senses the difference in radiant energy between an ambient reference (reference shutter blade) and the target (bearing). The resultant output is a signal which is proportional to the temperature rise of the bearing above ambient. This section describes how the HBD circuits operate to gather bearing heat data.

The advanced transducer or track circuit detects the presence of a train and informs the HBD to perform its pre-train scanner integrity test and open the protective shutters. The wheel gate transducers sense the presence of a moving wheel and produces a corresponding signal. The signals produced by the wheel gate transducers makes a timing circuit which keeps the reference shutters open during wheel passage. The reference shutters are only open while each wheel is in position to be scanned. With the reference shutter open the infrared energy from a bearing is focused on the sensor. The sensor converts the signal into a voltage which is amplified by the preamplifier circuit. This signal is fed to the peak hold circuit. A capacitor in the peak hold circuit is charged up to the peak value of the preamplifier output signal. The HBD software reads the value from the peak hold circuit via Analog to Digital converter (ADC) and saves the value for later processing.

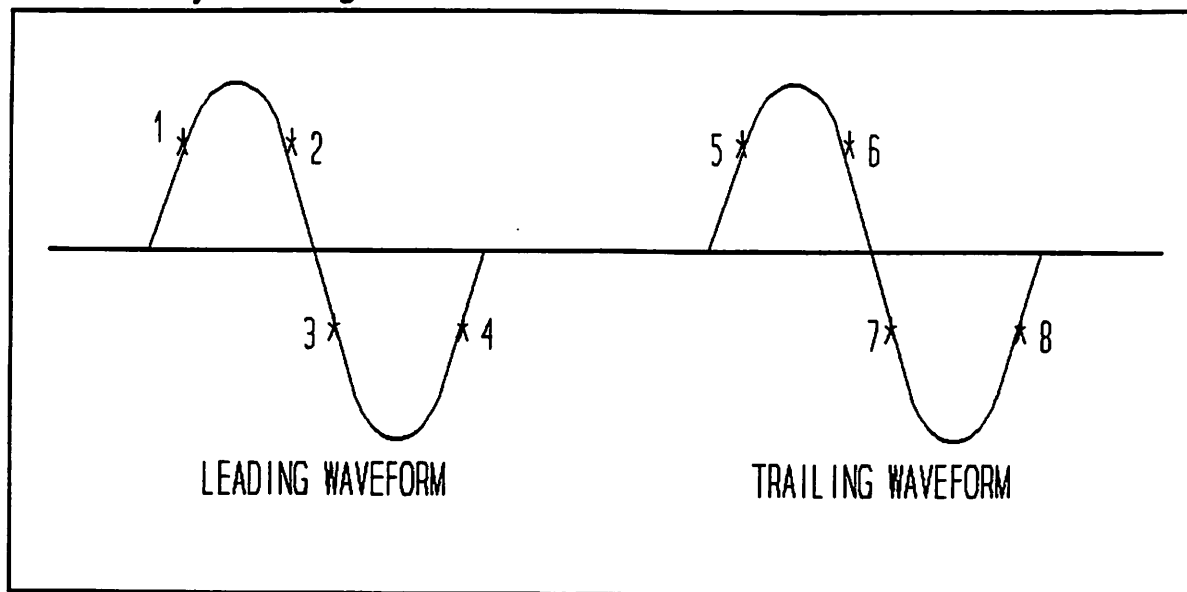
Start of Train

The advance transducer/track circuit initiates the start of train, by informing the HBD of presence of a train. The HBD starts the pre-train scanner integrity test and opens the scanner protective shutters. The protective shutters remain open until the End-of-Train Timeout. The End-Of-Train Timeout is reached when the HBD does not receive any gate interrupts for a period of 8 seconds (or when the track circuit goes down).

Wheel Gates

As a wheel traverses the wheel gate transducer, the reluctance of the magnetic path above the transducer is changed. This change in reluctance induces a voltage in the transducer coil that approximates one full cycle of a sine wave. The sine wave is converted to digital signals (interrupt signals) by comparators on the analog board. The HBD software uses the

converted digital signals as a timing mechanism to control the scanners, and AD conversion. The following figure shows the sine wave produced by the gate transducers, and the interrupt points created by the analog board.



The following paragraphs explain each interrupt cycle individually. Following is some of the terms used in this description:

Leading Waveform - The analog waveform generated by the leading transducer. This is the transducer which is first traversed by each wheel.

Trailing Waveform - The analog waveform generated by the second wheel gate transducer.

Each half cycle of the sine wave has two edges.

Leading Edge - The first half (leading edge) of the first cycle of the sine wave. This is the first interrupt point on the waveform.

Trailing Edge - The second half (trailing edge) of the first half of the sine wave (interrupt point 2).

Analog Board Circuits Used:

The following IC designators are for analog board II. The analog board I are given in the parentheses (Uxx). The operation description is given for channel 1, all other channels are the same with the exception of hardware addressing

The following analog board circuits are used to process the scanner heat values:

The *peak hold circuit* which consists of R94(R104), C54(C49), and OP Amp IC13(U28) receives its input from the IN5 network.

The *4 to 1 heat multiplexer* IC28(U25), receives the peak hold output and directs its output (CH1_PK and CH2_PK) to a 16 to 1 multiplexer.

Two *8 to 1 multiplexers* IC17(U26) and IC20(U27) combine to form a 16 to 1 multiplexer mentioned previously. The multiplexer gets its input from CH1_PK and CH2_PK of heat multiplexer IC28(U25), and directs its output to the ADC IC19(U21).

After *Analog to Digital Conversion* (ADC) IC19(U21) converts the analog data to a digital form, it activates the "DATA READY" output. This interrupt informs the HBD to get its heat information from ADC output which is port 1 of analog board.

IC29(U29) is the *discharge peak circuit* multiplexer. IC29(U29) is also used during train simulation, however when a real train is passing the detector, its only duty is to bleed the peak hold circuit.

Interrupt Point 1 (Leading Edge of the Leading Waveform)

During this period, the HBD opens the optical shutters on the preamplifiers. The optical shutters are controlled by bit 6 on port 2 (TB15-2) of the digital board. The HBD grounds this bit to force the optical shutters open. The optical shutters are closed at interrupt point 6. Figure 3 shows the relation between the optical shutters and the interrupt points on the transducer waveforms.

The HBD also inhibits the IC29(U29) heat multiplexer at this time, leaving a high impedance at the peak detector circuit (enabling peak hold circuit). Port 5 of the analog board is modified to xxxxxx10. Bit P5.1 disables the IC29(U29).

Interrupt Point 2 (Trailing Edge of the Leading Waveform)

The peak hold circuit is enabled (interrupt point 1). The IC28(U25) heat multiplexer is directed from -6 VDC to the heat channel, to set up peak hold measurements. To accomplish this the following steps are performed:

Port 5 is modified to xxx001xx. P5.4 enables the heat multiplexer IC28(U25). P5.2 and P5.3 point the peak hold output to the CH1_PK output of IC28(U25). The CH1_PK output is then routed to the ADC through 16 to 1 IC17(U26) and IC20(U27) multiplexer.

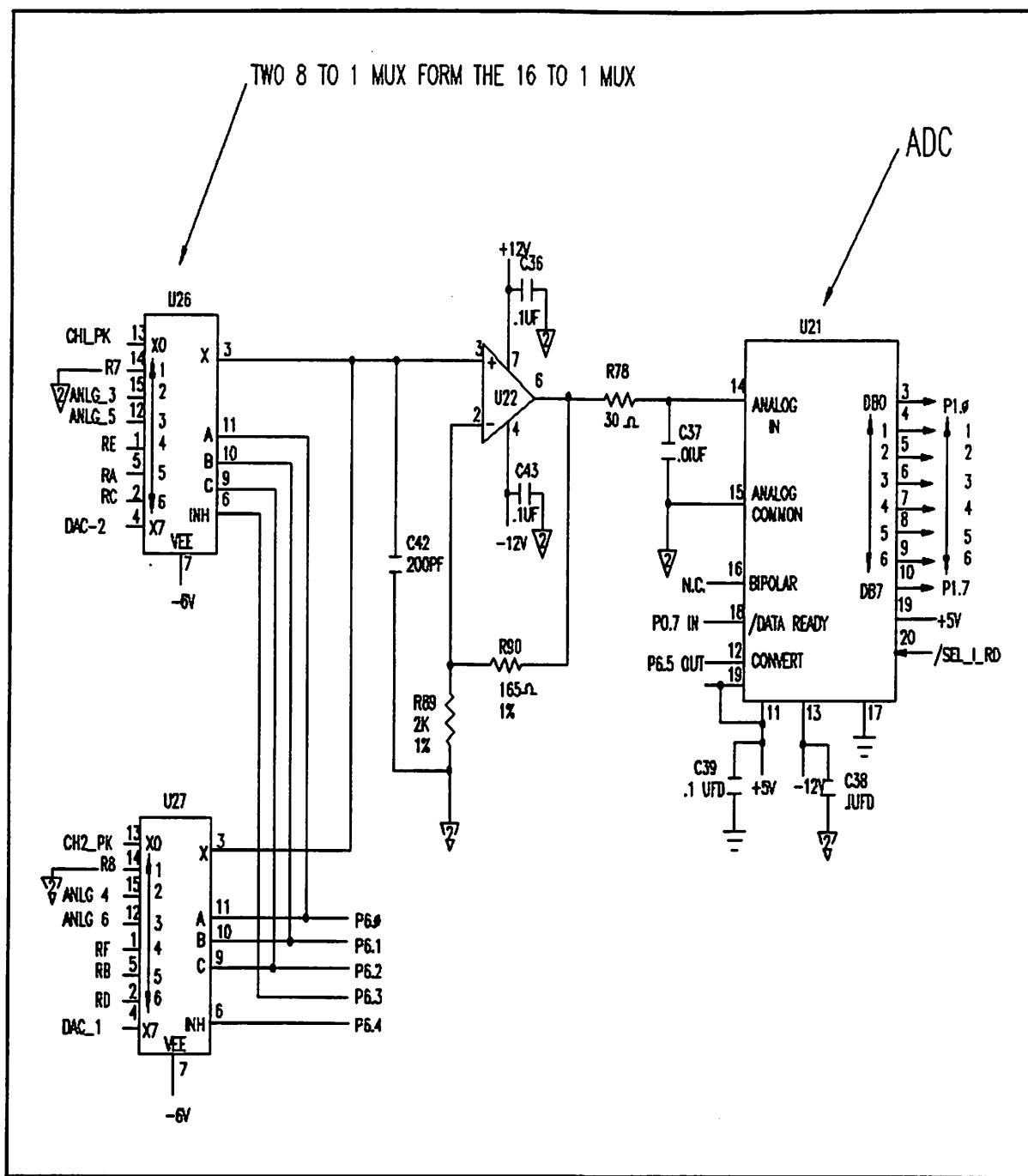
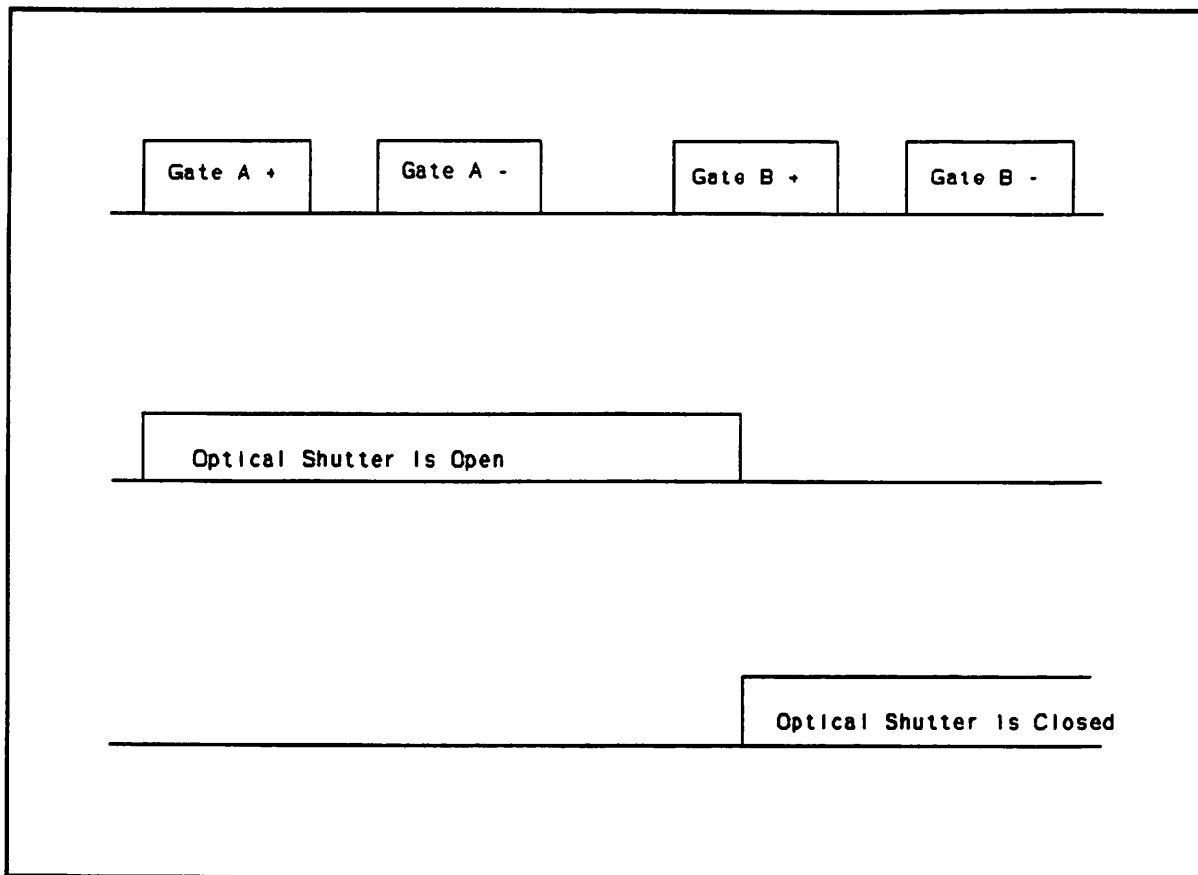


Figure 4

Interrupt Point 3

This interrupt is mainly used as a guard against noise on the cables. Interrupt point 3 verifies the sine wave as a true wheel gate waveform. If noise had generated the first two interrupt points, it should be gone by now. Interrupt point 3 indicates a valid transducer signal.



Interrupt Point 4

Not Used.

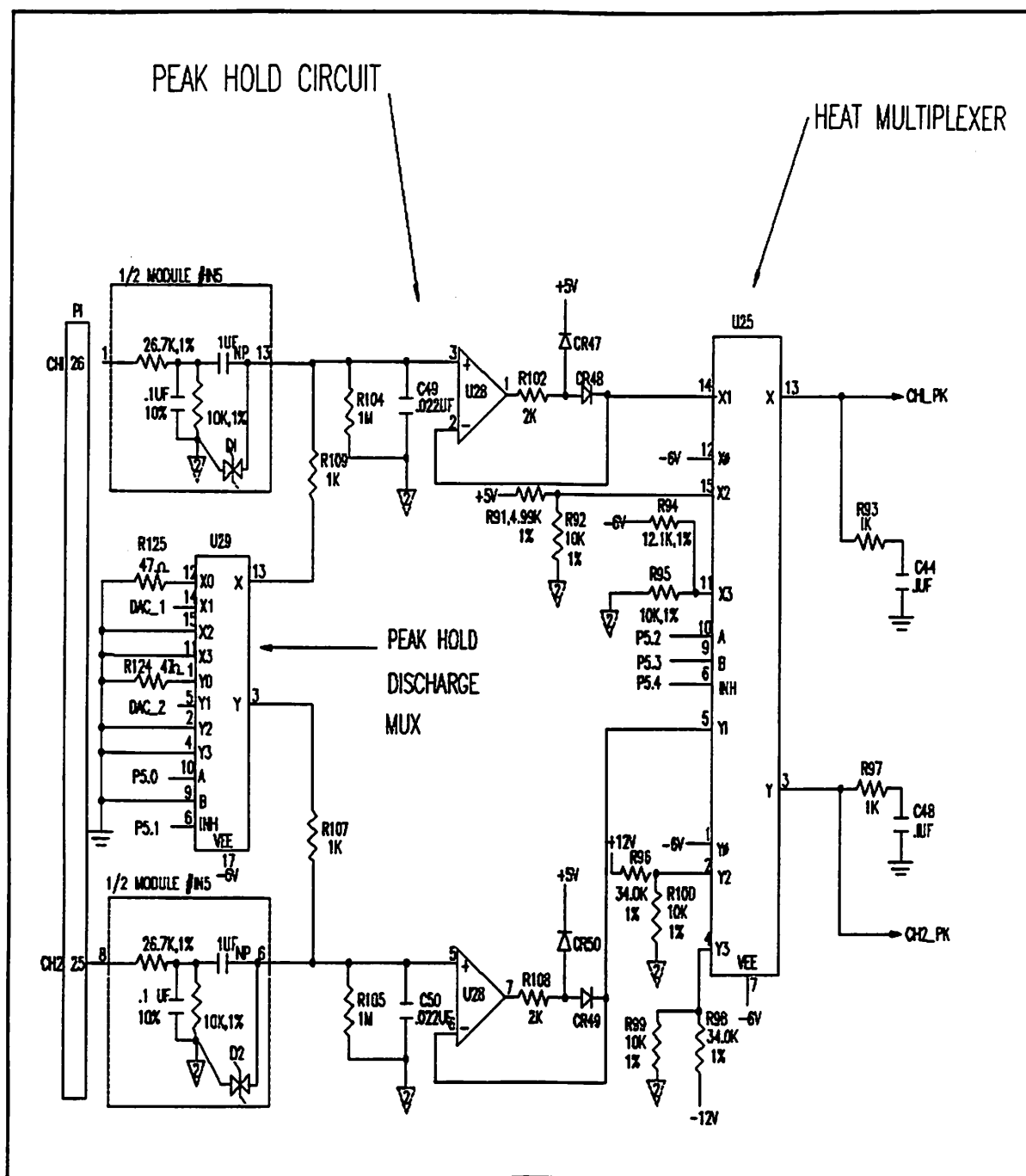
Interrupt Point 5 (Leading Edge of Trailing Waveform)

Not Used

Interrupt Point 6 (Trailing Edge of the Trailing Waveform)

The optical shutters are forced closed at this time. To do this bit 6 of port 2 (TB15-2) on digital board is cleared.

Next the peak hold capacitor is connected to the AD buffer by modifying port 6 of the analog board to xxx110000. Bits P6.0, P6.1 and P6.2 select CH1_PK which is the output of peak hold through heat multiplexer IC28(U25). P6.3 enables the multiplexer IC17(U26), while P6.4 disables the second multiplexer IC20(U27). This allows the CH1_PK (channel one heat value) to reach the ADC IC19(U21). Please note that at this time the HBD is processing channel 1 heat. After reading channel 1 heat, these steps (interrupt point 6) is repeated once more to read channel 2 heat. Port 6, however, is modified to xxx0,1000, disabling the first multiplexer and enabling the second multiplexer. This allows channel two heat to reach the



ADC. These commands take approximately 5 microseconds to allow the AD buffer to stabilize.

After the HBD has directed the channel heats to the ADC, it modifies port 6 to xx1xxxxx. P6.5 is the "Start AD" input of ADC IC19(U21). P6.5 only needs to be high for a very short period of time. The HBD clears P6.5 immediately (after four clock cycles). The HBD is now ready to read the ADC output. The HBD delays a maximum of 3.44 millisecond for the conversion to be completed. If the AD conversion was successful, the

HBD receives an interrupt from the analog board port 0 bit 7 (P0.7 is the "DATA READY" output of ADC IC19(U21)). If the HBD does not receive an interrupt within 3.44 milliseconds, it uses a value of zero for the channel heat.

After the ADC ready interrupt has been received the HBD reads and stores the heat value for the current channel. The heat value is read from AD data port, which is port 1 of the analog board.

The above procedure is repeated three more times to get the heat values for channel 2, 3, and 4. Note: Channel one and two use the first analog board (address FF40 hex), and channel 3, and 4 use the second analog board (address FF50 hex). The only difference is modifying port 6 of analog board. Bits p6.3 and P6.4 determine which channel uses the ADC.

Writing Heat to the Chart Recorder

The HBD invokes the "analog" function once every 2.5 milliseconds during the passage of a train, real or test. This function looks for a new axle. If a new axle has been added to the buffer by the above procedure the heat values for channel 1 and 2 are retrieved from the buffer and directed to the chart recorder. This function first evaluates the heat values. If the heat values are less than zero, nothing is output to the chart recorder and the positive heat values are printed on the chart recorder in form of vertical bars.

Chart recorder paper is divided into two sections. The top section is used for channel one heat values, and the bottom section is used for the channel two heat values and end-of-train data logging. Each section of the paper is then divided into 25 equal parts (increments) with each increment representing one millimeter of heat. The HBD prints vertical bars for heat values in the range of 1.6 mm and 25 mm. The HBD does not print negative heat values. The negative bars (vertical bars under the zero reference line of each section) are used for car recognition indication and train reversal.

Processing Heat Values

The "analog" function previously mentioned is also responsible for processing the heat values (alarms). After writing the heat value to the chart recorder, it performs the "absolute alarm analysis" on the new axle. The analog function then checks for a minimum of 6 axles and starts trying to recognize a car. If the car recognition was successful, "carside alarm analysis" is performed on that group of axles. If the car recognition does not identify a car from the available axles, the "simple/single alarm analysis is performed". The results are stored in the axle buffer, to be transmitted to the DCP.

Transmitting Heat Data to the DCP

After the car recognition procedure has been accomplished the HBD transmits the axle data to the DCP. The number of axles transmitted to the DCP depends on the outcome of the car

recognition. If the car recognition failed, only one axle is transmitted. If the car recognition was successful, all the axles belonging to the car are transmitted to the DCP. The transmitted information for each axle consists of :

Heat Alarms : Bit encoded, showing heat alarms

AUX Alarms : Bit encoded, showing AUX alarms

Axle Status : Car recognition flags

Ch1 Heat : Hot box 1 (DAC1)

Ch2 Heat : Hot box 2 (DAC2)

Ch3 Heat : Hot wheel 1 (DAC3)

Ch4 Heat : Hot wheel 2 (DAC4)

Spacing : time interval between current axle and previous axle.

Speed : Speed of the axle (current speed of train).

Scanner Integrity Test

An integrity test is performed on the scanners at the time a train is detected. The exact scanner test procedure varies for each type of scanner since some scanners have protective shutter switches, etc. The types of scanners that have integrity tests performed on them are the Harmon Electronics, Inc. Model 32 and Model 32R, and all scanners manufactured by Servo Corporation of America. GE scanners do not have an integrity test performed. Refer to figures 1 through 4 illustrating scanner configurations and circuitry tested.

The scanner integrity test is called from the main program and is executed every fifty milliseconds. Each time this routine is called, one step of the integrity test is performed. Built in delays are used to allow the protective shutters to open before they are tested for operation. The entire integrity test takes approximately 750 milliseconds to perform.

The integrity test is initiated when an approaching train passes over an advance transducer or closes an approach track circuit. The integrity test is broken up into 15 different steps that are performed in fifty milliseconds intervals. Following is a step by step description of what is performed during each step of the integrity test. If the system has Harmon Electronics, Inc. hot wheel detector scanners installed, all steps performed for the hot journal scanners will be duplicated for the hot wheel scanners. If a state has a "Do nothing" comment in the description this state has been installed to allow the protective shutters time to open, and the switches time to stabilize before a critical test is performed.

The actual procedures that read the heat from the scanners is described in detail in the "Scanner Heat" section of this manual. Refer to that section for more information concerning the hardware/software interface.

Step 1

- If the scanner is manufactured by Servo Corporation of America the integrity test proceeds to step 5.
- For scanners equipped with Model 38 or Model 3800 preamplifiers the integrity test lamp relay drive output is activated. Activating the integrity relay provides an input to the Model 38 preamplifier that turns on the integrity lamp. The integrity lamp is used to saturate the pyroelectric device that reads the infrared heat from the passing railcar journal. If a Model 3800 preamplifier is installed the integrity lamp input is a signal that turns on the IRIS and prepares it for the train that is about to be scanned.
- The optical shutters are closed. A optical shutter is used in the Model 38 preamplifier as an optical reference. This shutter must be in a known position before the start of the integrity test. The Model 3800 IRIS uses a rotating optical reference. The position of the rotating reference is known at all times.
- The protective shutter inputs are tested to see if the protective shutters are closed. If the protective shutter is open after this test is completed a "Protective Shutter Stuck Open" warning is generated.

Step 2

- Do nothing. A "do nothing" state causes a fifty millisecond delay that is provided so that the scanner inputs are allowed to settle before they are tested.

Step 3

- Do nothing.

Step 4

- Do nothing.

Step 5

- Do nothing.

Step 6

- If Model 38 or Model 3800 preamplifiers are being tested the integrity test precedes to step 7.
- If a Servo bolometer is being tested the integrity relay is activated placing a 100 Ω resistor in series with -200 VDC. This makes +200 VDC and the -200 VDC unbalanced producing a "heat" pulse out of the bolometers.
- The analog circuitry is prepared to start processing the "heat" pulse generated by the bolometer.

Step 7

- If the scanners being tested are Servo scanners the "heat" pulse is processed by the analog board and is converted to a digital value.
- Turn off the integrity test lamps.
- Go to step 8.
- If Model 38 or Model 3800 preamplifiers are being tested prepare the analog circuitry for the incoming heat pulses.
- Start opening the optical shutter, or in the case of the Model 3800 preamplifier that does not have an optical shutter this signal is used to tell the IRIS to send the results of the last integrity test to the HBD. This is not a heat pulse as it is in the Model 38 preamplifier but is a "go" or "no go" signal.
- Wait approximately 4 milliseconds and then stop the optical shutters.
- The heat pulse is processed by the analog board and is converted to a digital value to be used to determine if the preamplifier is working correctly.
- Close the optical shutters. This step tests the performance of the optical shutter. If the shutters do not open fast enough an integrity failure will be

- generated stating that the preamplifier is bad.
- The heat pulse obtained from the scanner is then written to the chart recorder. This is the first integrity pulse.
- The heat pulse value is compared to the "High Limit" threshold setting. If this value is less than the "High Limit" a bad preamplifier message is generated.

Step 8

- If Model 38 or Model 3800 preamplifiers are being tested prepare the analog circuitry for the incoming heat pulses.
- Start opening the optical shutter. See step 7.
- Wait approximately 2 milliseconds and then stop the optical shutters.
- The heat pulse is processed by the analog board and is converted to a digital value to be used to determine if the preamplifier is working correctly.
- Close the optical shutters. This step tests the performance of the optical shutter. If the shutters do not open fast enough an optical shutter marginal warning will be generated stating that the preamplifier is bad. This value is meaningless if it is generated by the IRIS since the optical shutter cannot be tested. If this pulse is not present with an IRIS installed there is a wiring problem since the IRIS always generates a full scale pulse for this test.
- The heat pulse obtained from the scanner is then written to the chart recorder. This is the second integrity pulse.
- Compare this value to the "High Limit" threshold setting. If this value is less than the "High Limit" the optical shutter marginal message is generated.
- Turn off the lamps.

Step 9

- Write the heat to the chart recorder.

Step 10

- Write the heat to the chart recorder.

Step 11

- Do nothing.

Step 12

- Do nothing.

Step 13

- Do nothing.

Step 14

- Test the protective shutter input circuitry to see if the protective shutter is open. If the protective shutter is stuck closed an integrity failure will be generated.

Step 15

- The integrity test is "turned off" so that the main program will not continue to perform the integrity test. The results of the integrity test are made available to the main program so that they can be provide to the speech processor and the DCP.

Wheel Transducers

Main Board Utilized

ANALOG BOARD

Theory Of Operation

The Wheel Transducer (WT) is a passive device that synchronizes trackside equipment operation to the wayside equipment to perform heat analysis. The output of the Wheel Transducer is a single sine wave with its period and amplitude being a function of train speed. Note: If the wiring (polarity) of transducer is reversed, the output is a cosine wave which will disrupt the operation of HBD.

The HBD must be equipped with either a track circuit or two wheel transducers (advance transducers) for system turn on. Advance transducer duties are twofold:

1. Inform HBD of arrival of a train (system turn on).
2. Determine train direction.

The HBD must also be equipped with two additional wheel transducers, referred to gating transducers. The gating transducers provide the HBD with a timing mechanism to control scanners, sample heat, and compute train speed and axle spacing.

The analog signals from the transducers are converted to digital signal via analog board circuitry. The converted digital signals then interrupt the HBD software to perform heat analysis.

Transducer Terminology

The following terms are used to describe transducer signal processing.

- a - **LEADING WAVEFORM** - Sine wave from the gating transducer which is first traversed by each wheel.
- b - **TRAILING WAVEFORM** - Sine wave from the second gating transducer.
- c - **LEADING EDGE** - Rising edge of one half cycle.
- d - **TRAILING EDGE** - Falling edge of one half cycle.
- e - **TRANSDUCER A** - The transducer to the south/east of the second transducer (also called first transducer).

f - *TRANSDUCER B* - The transducer to the north/west of the first transducer (also called second transducer).

g - *DIRECTION 1* - Train direction if the train is travelling from transducer A to B.

h - *DIRECTION 2* - Train direction if the train is travelling from transducer B to A.

IC Designators

The IC designators used are for analog board II. The analog board I are given in the parentheses in the form (Uxx).

Analog Circuits Used

One of the HBD features is to simulate passage of a real train to test the integrity of system. The test train multiplexer IC16(U5) of the analog board is a major component used in the simulation unit. By enabling IC16(U5), the DACs can be pointed to one of the advance or gating transducer circuits. Upon receiving an interrupt from the transducers (gating or advance), the input status of the test train multiplexer is examined to determine whether the interrupt belongs to a real train or a simulated train. P5.7, the inhibit input of IC16(U5), is examined. If P5.7 is at logic high, the IC is disabled, the interrupt belongs to a real train. The logic for processing real and test trains is the same. However, the train type must be determined for proper control of the radio and for transmitting train data to the DCP.

BD_INT is the interrupt line.

Port zero (P0) of the analog board informs the HBD as to which transducer interrupted the software. P0 is controlled by the trackside equipment. P0.0 and P0.1 are used by gating transducer A, while P0.2 and P0.3 are used by gating transducer B. P0.4 is used by advance transducer A, and P0.5 is used by advance transducer B. P0.6, and P0.7 are not currently used.

Port 3 and 4 of the analog board are used by the HBD software to control the sequence of transducer interrupts. This is used as protection against possible noise from the transducers, polarity reversal, and train change of direction. P3.0 and P3.2 allow gating transducer A to interrupt the software (enabling NAND gates IC23A(U6A), and controlling IC23C(U6C) for the rising or falling edge of the sine wave). P3.3 and P3.5 are used to enable/disable the interrupts from gating transducer B. P4.0 controls the interrupts from advance transducer A, and P4.2 controls the interrupts from advance transducer B.

Interrupt Priorities

Although the advance and gating transducers use the same line to interrupt the software, gating transducers have been given a higher priority. When the software is interrupted by P0 (used by gating and advance transducer), the Least Significant Nibble (LSN) of P0 is

examined first. P0 LSN is used by the gating transducers. After processing the gating transducer interrupts the Most Significant Nibble (MSN) of P0, which is used by the advance transducers, is examined.

Software Terms

The following terms are used for the discussion of transducer signals (*italic font is used to distinguish these terms*).

- a - *TIMER 1* - Used to measure the time interval between two consecutive wheels to reach the same gating transducer. This timer is used to calculate the axle spacings.
- b - *TIMER 2* - Used to measure the time interval for one wheel to travel from one gating transducer to the other. This timer is used to calculate train speed.
- c - *GATE TRANSDUCER A COUNT* - A counter for the rising edge interrupt of gating transducer A.
- d - *GATE TRANSDUCER B COUNT* - A counter for the rising edge interrupt of gating transducer B.
- e - *REVERSE TRANSDUCER A COUNT* - A counter for polarity reversal of gating transducer A.
- f - *REVERSE TRANSDUCER B COUNT* - A counter for polarity reversal of gating transducer B.
- g - *AXLE COUNT* - The number of axles for the passing train. Axle count does not necessarily equal to gate transducer counts. Axle count is incremented when all the expected interrupt points have been received by HBD.
- h - *TRANSDUCER INTERRUPT ERROR FLAG* - The error flag is set, if gating transducer interrupts are out of order. This flag is used to issue a warning/error during End Of Train timeout.

Status of Ports Before Train Arrives

The 'x' used in the masks refers to don't cares. These bits are either controlled by other tasks, or not used.

Port 4, which controls the advance transducers interrupts, is set to xxxx0101. P4.0 and P4.2 enable NAND gates IC27D(U8D) and IC27C(U8C) allowing the advance transducers to interrupt the software. P4.1 and P4.3 are set to zero causing the rising edge of the sine wave to be expected by the HBD.

Port 3, which controls the gating transducers interrupts, is set to xx011011. As described later, this value is modified depending on current train direction. The default value is the safety net in case the advance transducers are dead/faulty. P3.0, P3.1, P3.3, and P3.4 at logic high, allows both gating transducers to interrupt the software.

Advance Transducer Interrupts

The output of the advance transducers is a single sine wave with the zero crossing occurring when the wheel is centered over the transducer. The sine wave goes through the negative comparator IC26(U2). The comparator output goes through XOR gate IC24A(U7A) /IC24B(U7B), and then to the NAND gate IC27D(U8D)/IC27C(U8C) and P0 of analog board. P4.1 and P4.3 determine whether the comparator output is sent through directly, or inverted. These components convert the sine wave into two interrupt points, as shown in figure 1.

As shown in figure 1, the negative portion of the sine wave is not used. As described later in this section, the same is not true for gating transducers. Since the gating signals play a critical part in heat processing the negative half of sine wave is used to verify a proper signal from the

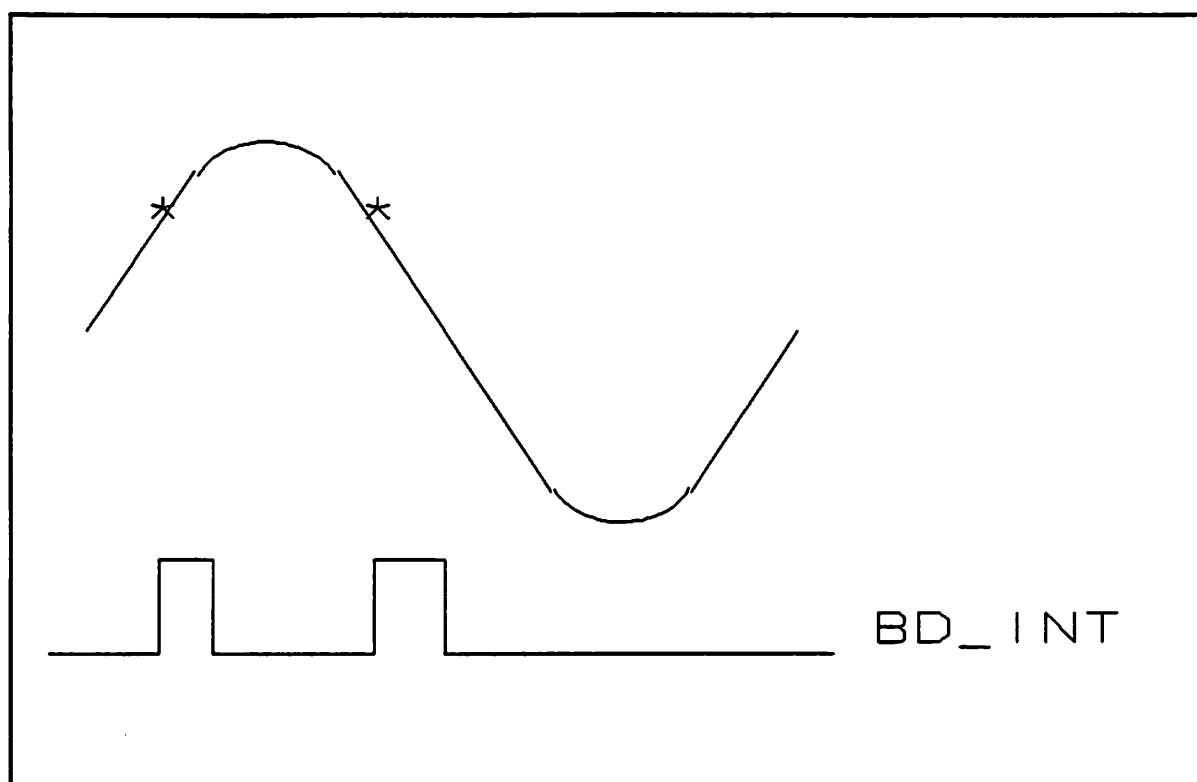


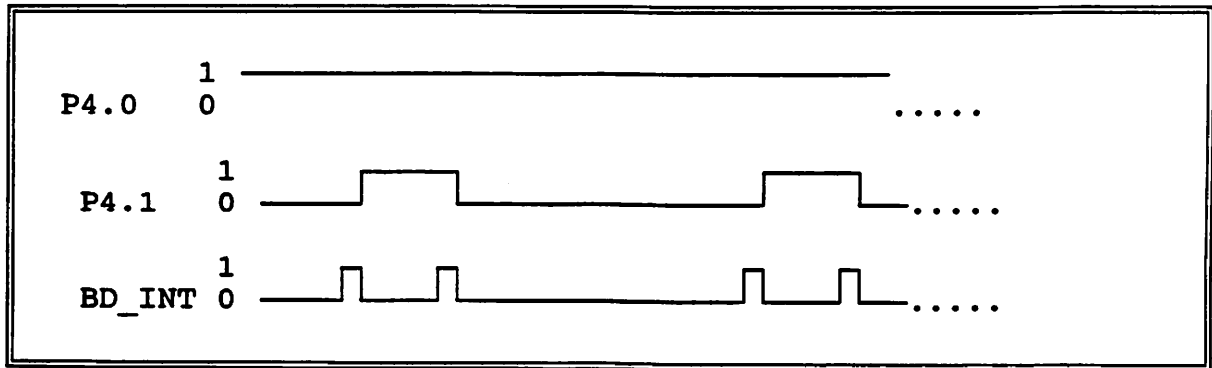
Figure 7 Advance transducer sine wave is converted into two interrupt points

transducers.

Port 4 is used to control the interrupt points. For example if P4.1 is cleared (logic zero), the rising interrupt is enabled. But if P4.1 is set to one, then the falling interrupt is enabled. Note: P4.0 is high allowing the NAND gate IC27D(U8D) to interrupt the software.

Since both the rising and falling interrupts use P0.4, P4.1 is used to distinguish between the two

interrupts. Although P4.0 is kept high at all times (leaving the NAND gate enabled), P4.1 is toggled on each interrupt point. The following diagram shows the proper sequence of interrupts from the advance transducers.



Processing Advance Transducer Signals

The HBD software can be configured to operate in one of the following modes:

- a - Use track circuits (advance transducers are not present).
- b - Use advance transducers for system turn on only.
- c - Use advance transducers for system turn on, and train direction.

For configuration (a) port 4 is modified to xxxx0000, disabling all the interrupts from the advance transducers. Although the signals from the advance transducers (or noise) are passed to P0, the software does not examine the status unless interrupted via BD_INT. Disabling NAND gates IC27C(U8C) and IC27D(U8D) disables the advance transducer interrupts.

Most HBD software has been configured to use the advance transducers for system turn on and train direction.

The Interrupt Service Routine (ISR) first examines P0.4 to determine if the interrupt belongs to advance transducer A. If P0.4 is set section "ADVANCE A INTERRUPTED HBD" is executed. P0.5 is then examined for any possible interrupts from the advance transducer B. Section "ADVANCE B INTERRUPTED HBD" is executed, if P0.5 is set.

Note: It is possible for both advance transducers to interrupt the HBD at the same time. or example, one end of train can reach advance transducer B, while the other end is still at the advance transducer A.

Advance A Interrupt (p0.4 is high)

P4.1 is examined to determine whether the interrupt is from a rising or falling edge. As described previously if P4.1 is zero the interrupt belongs to the rising edge.

If the rising edge has interrupted the HBD step 1 is executed. If the falling edge has interrupted the HBD (P4.1 is one), then control is passed to step 2.

1 - At this point, IC16(U5) is examined to determine whether the interrupts are from a real train or simulated by the HBD DAC circuits for a test train. Note: Port 5 of analog board is write only. Port 5 shadow (software variable same as port 5 settings), is examined to determine IC status. For a test train P5.5, P5.6, and P5.7 should be 011xxxxx, where P5.7 enables the IC, and P5.5 and P5.6 direct the DAC to the advance transducer circuit. If the interrupts are from a real train and this is the first interrupt from the advance transducer, a special routine is called which performs the pre-train housekeeping. The *start up* routine performs the following functions.

- a - Execution of front panel functions are canceled, such as test train, chop, data recall, board self test, etc.
- b - Train processing variables are initialized; such as, number of axles and cars, train speed and direction, warning and error codes, highest and lowest heat readings, etc....
- c - Start of train message is transmitted to DCP.
- d - The pre-train integrity test is started.

At this point (after execution of *start up* routine), the *gating transducer counts* are examined. If both are still zero the train has not reached the gating transducers. In this case, a timer is set to 10 seconds. When the timer expires the HBD goes into the End Of Train timeout. This timer is mainly controlled by the gating transducers. When an axle approaches the gating transducers the timer is set to 10 seconds. As long as the train has not reached the gating transducers the advance transducers perform the duty of setting the timer to 10 seconds preventing the HBD from going to End Of Train timeout.

If train direction has not been set yet the following steps are performed to set the train direction. If the first interrupt is from advance transducer A direction 1 is set (TB12-1, P1.0 of digital board is grounded). If the first interrupt is from advance transducer B, direction 2 is set (TB12-2, P0.1 of digital board is grounded).

Gate sequence is set to one. The *gate sequence*, as described earlier is a software control for gating transducer interrupts. Gate sequence is clearer when we discuss gating transducer interrupts.

Port 3, which is used to enable/disable gating interrupts, is set to 00011111. This bit pattern indicates that the positive and negative pulses from leading transducer, and the positive pulse

from trailing transducer are enabled. Although the first logical interrupt must be from the rising edge of the leading waveform, other interrupts are enabled for polarity checking and diagnostics.

The steps described above are only performed one time after receiving the first interrupt from the advance transducer. The following operations are performed for each interrupt received from advance transducer A.

Advance transducer A count is incremented. After incrementing the variable port 4 is set to xxxxxx11. P4.1 is set to one, indicating that the next interrupt should be the falling edge of the sine wave.

2 - This step is performed when advance A trailing edge (second interrupt point) has interrupted the HBD. The only operation at this point is modifying port 4. Port 4 is set to xxxxxx01. P4.0 is one, enabling advance transducer A interrupts. P4.1 is set to zero, indicating that the next interrupt belongs to the rising edge of the sine wave (the negative half does not generate an interrupt).

Advance Transducer B Interrupt (p0.5 is set)

Processing the signals from advance transducer B is same as advance transducer A. Different masks and input bits are used to process the advance B interrupts. The following briefly describes the different masks used in processing advance transducer B (refer to "ADVANCE TRANSDUCER A INTERRUPTED HBD" for a more detailed discussion).

P0.5 is examined to determine if advance transducer B has interrupted the software. P4.3 is used to determine whether the interrupt belongs to the rising or falling edge of the sine wave.

When executing step 1, direction 2 is set (TB12-2, P1.1 of digital board) and *advance transducer B count* is incremented.

Port 3 is set to 0011,1111. Finally port 4 is modified to xxxx11xx, indicating the next interrupt from advance B is the falling edge of positive half.

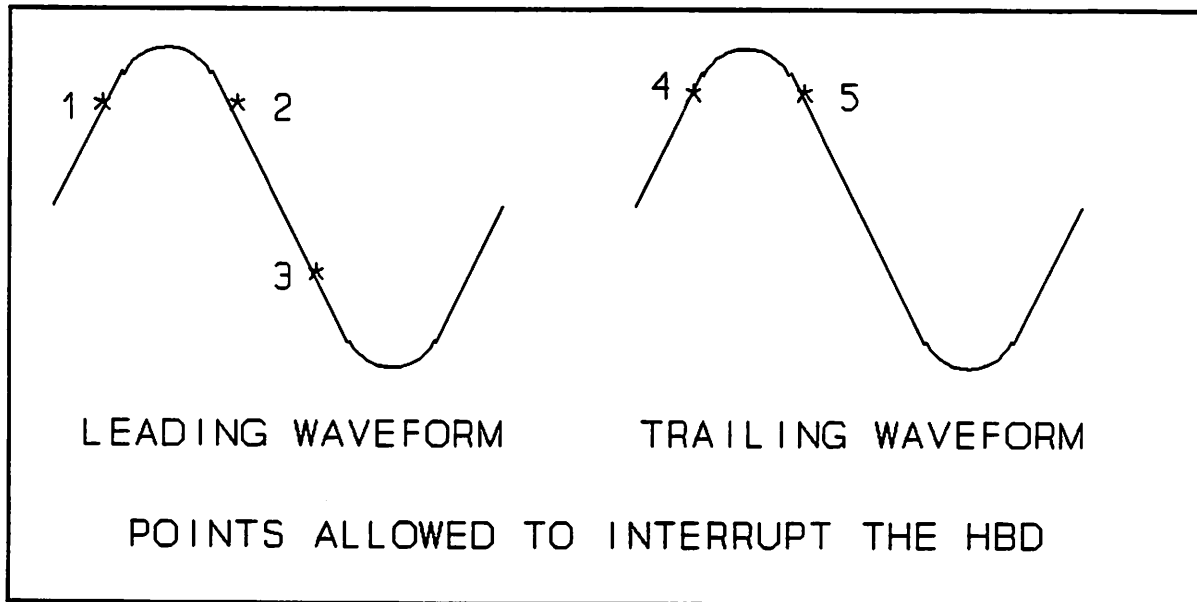
When executing step two, port 4 is modified to xxxx01xx, indicating the next interrupt from advance B is the rising edge of the sine wave.

Advance Transducers at End of Train Timeout

Upon train departure the *advance transducer counts* are compared. If the difference between the counts is 5 or more, a warning message is written to the chart recorder (ADV_X_A_XXX ADV_X_B_XXX, where 'xxx' are the actual counts). Refer to the "HBD ERROR MESSAGES" for more information about the warning message.

Gating Transducer Interrupts

Gate sequence is defined as a tool to manage the gating transducer interrupts. As shown in the following diagram, the gating transducers interrupt the HBD in five points (these are the only interrupts allowed by the HBD software).



Gate sequence is used to keep track of which interrupt should occur next, versus the actual interrupt which is active. This technique helps to check for faulty/dead transducers, polarity reversal, change of direction, and noise. For simplicity, processing transducer interrupts is divided in five sections, one for each interrupt point. Depending on the current value of *gate sequence*, only one of these sections is executed at any given time.

Processing the First Signal From Gating Transducers.

Upon receiving the first interrupt from the gating transducers, the following steps are performed.

- a - System status is checked, to make sure the advance transducers have started the system (pre-train housekeeping).
- b - If the system has been started, the following steps are bypassed, otherwise the following steps are executed.
- c - The *start up* routine is executed. The *start up* routine performs the following functions.
 - * Execution of front panel functions are canceled, such as test train, chop, data recall, board self test, etc..

* Train processing variables are initialized; such as, number of axles and cars, train speed and direction, warning and error codes, highest and lowest heat readings, etc..

* Analog board IC16(U5) is examined to determine whether the current interrupt is from a real train or the HBD simulated train.

* Start of train message is transmitted to DCP.

* Integrity failure is announced, since the HBD did not have time to perform the pre-train integrity test.

d - Direction 1 and direction 2 are examined. If no direction has been set, or the advance transducers are not present (software configuration), train direction is determined. If the interrupt is from gating transducer A, direction 1 is set. If the interrupt is from gating transducer B, direction 2 is set.

Although steps a, b, and c are only executed once (first interrupt from gating transducer), step d is performed until the HBD can determine the correct direction of passing train. At that time step d will also be bypassed.

If the train direction cannot be set by the first signal from the gating transducers, the following guidelines are used until a direction is determined. Direction 1 is set if the interrupt is from the rising edge of leading waveform transducer A. Direction 2 is set if the interrupt belongs to the rising edge of leading waveform transducer B.

The rising edge of gating transducer A interrupts the HBD if P3.0 and P3.1 are both set to one. Therefore if the gate sequence is one, and both bits are one, direction 1 is set. The rising edge of gating transducer B interrupts the software if P3.3 and P3.4 are both set to one. Therefore, if gate sequence is one, and both bits are one, direction 2 is set. Note: Gate sequence must be one. No other section of the ISR determines train direction.

It is possible for the HBD to set both directions, or no direction at all. This is due to the faulty transducers, reverse wiring, or analog board failure. In this case an error/warning message is written to the chart recorder and integrity failure is announced (if analog board is faulty). Refer to the "HBD ERROR MESSAGES" for more information.

Interrupt Service Routine

The gating transducer Interrupt Service Routine (ISR), is called when any of the advance/gating transducers interrupt the software (via BD_INT). First the Least Significant Nibble of P0 is examined for any gating interrupts. P0.0, P0.1, P0.2, and P0.3 are the gating transducer interrupt points. If there is an active gating interrupt one of the following sections is executed. The *gate sequence* determines which section processes the interrupt. After processing the gating interrupt or if there are no active gating interrupts, control is passed to the second part of the

ISR. The Most Significant Nibble of P0 is examined for any active advance interrupts (P0.4 and P0.5).

Processing advance interrupts was discussed in the previous section. The following sections describe how gating transducer interrupts are processed. Each section starts with a brief description of which interrupts are enabled, and which interrupt should occur.

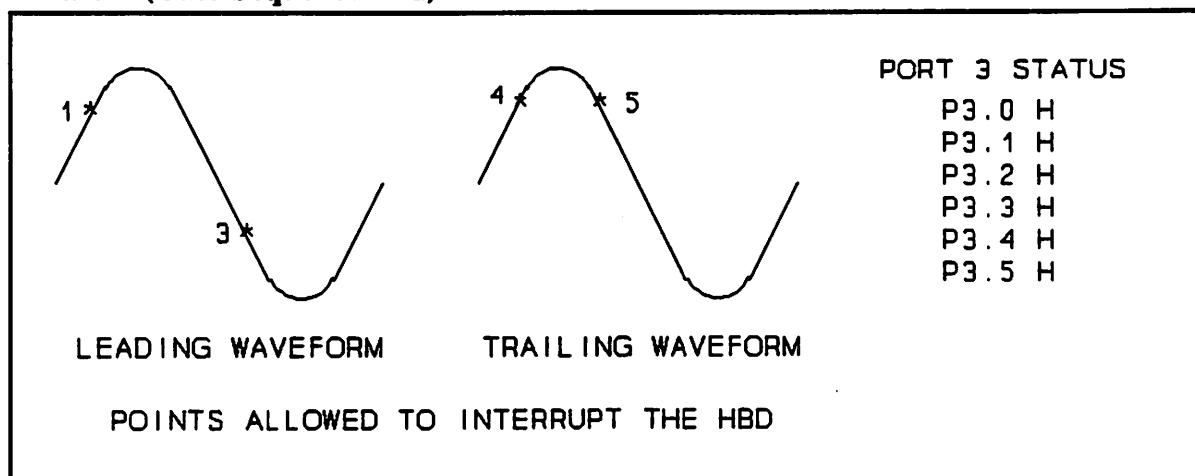
Unlike advance transducer interrupts the sections which process the gating transducer signals perform extensive error checking on the incoming signal. There are three source of errors that are checked.

1. - Noise creating interrupts
2. - Polarity reversal
3. - Loss of interrupts

Each section consists of several steps. **Note: After performing the operations in the specified step, control is passed to second part of the ISR, where advance transducer interrupts are processed. At each stage, only one step is executed.**

Each section consists of two parts; one for direction 1, and one for direction 2. The first part explains in detail, the logic for processing the interrupt. The second part only briefly describes the different masks and inputs used for direction 2. Each section also starts with a figure which demonstrates which interrupts are enabled. **Note: The figure is for direction 1 only.**

ISR Part 1 (Gate Sequence = 1)



This section processes the leading edge of the leading waveform (interrupt point 1). At this time the positive half from both gating transducers and the negative half of the leading transducer are enabled (port 3 is at xx011111). Leaving both positive halves enabled checks for train direction reversal, while the negative half of the leading transducer is for polarity reversal. For normal operation the only incoming interrupt should be the rising edge of the leading transducer (P0.0 for direction 1, and P0.2 for direction 2).

The *timeout timer* is set to 8 seconds. The HBD enter the "End Of Train Timeout" when this timer expires. There is always 8 seconds between the last axle of train and HBD End Of Train Timeout.

At this point, depending on train direction, one of the following sections is executed. Note: The logic for both directions is the same; different masks are used to verify the correctness of current interrupt and enabling the next logical interrupt.

If both directions have been set, section "Direction 1" is executed. If none of the directions have been set, none of the following sections is executed (interrupts are out of order, interrupt controls are re-initialized, so that the next interrupts can be captured properly).

Each section examines the sequence of interrupts to determine if the current interrupt is in proper order or noise has created out of phase interrupts.

Direction 1

(Axles are traversing transducer A first). Since the gate sequence is 1, the correct interrupt must be interrupt point 1. Therefore P0.0 is examined first. If the interrupt is from P0.0, and P3.1 is also set to 1 (rising edge), step 3 is executed (step 1 and 2 are for processing advance transducer interrupts). At the end of step 3, gate sequence is set to 2. For the next interrupt, the second section of ISR, which processes the falling edge of leading waveform, is executed.

If the interrupt is not from the transducer A (leading waveform), step 4 is executed. Step 4 consists of several guidelines which determine the proper error/reversal operations to perform. Step 4, which is the error checking logic, does not change the *gate sequence*. Thus section one of ISR (this section) is executed again. By taking this approach, the HBD will wait for the next wheel to set the interrupts back in their logic positions.

3 - Interrupt point 1. *Gate transducer A count* is incremented and port 3 is modified to xx000001. The new port enables NAND gate IC23A(U6A) and disables the rest of the interrupt control gates. P3.1 is set to 0. The next valid interrupt is the falling edge of the sine wave from transducer A. The *gate sequence* is also set to 2. At this point, *timer 1* (used for axle spacing) and *timer 2* (used for train speed) are initialized.

During this period the optical shutters are opened by grounding TB15-2 (digital port P2.6). The heat multiplexer IC29(U29) is also inhibited by setting port 5 to xxxxxx10 (P5.1 disables the IC29(U29)). Disabling the heat multiplexer leaves a high impedance at the peak hold detector circuit (enabling the peak hold).

At this point processing the gating interrupt is finished. Control is passed to step 1, where advance transducer interrupts are processed (if any).

4 - This step is executed if the correct interrupt was not received. The following guidelines are used to determine the source of interrupt. The possible interrupt sources include: rising edge

of transducer B, negative half of transducer A, and noise. After executing the proper step control is passed to step 1 to examine the advance transducer interrupts (they also use P0 of analog board). Note: The following steps are performed in a sequential manner until the correct step is found. Since the current interrupt is out of order the *gate sequence* is not changed.

* First check for an interrupt from the positive half of transducer B (P0.2). If P0.2 is one, then P3.4 is examined, to determine whether the interrupt belongs to the rising or falling edge of positive half. If P3.4 is one (rising edge) step 5 is executed, otherwise (falling edge) step 6 is executed.

* P0.1 is examined, to determine whether the negative half of transducer A is source of interrupt. If P0.1 is one, P3.2 is examined. P3.2, which is controlled by the software, indicates whether the interrupts from P0.1 are allowed or not. If P3.2 is one, step 7, which performs the reversal polarity logic, is executed, otherwise step 8 (errors on interrupts) is executed.

* If all the tests mentioned fail, step 8 is executed. The only interrupts which are not checked are:

** Negative half of transducer B.

** Falling edge of transducer A.

5 - (P0.2 = 1, P3.4 = 1) This is the rising edge interrupt from transducer B. If this is the first signal from the transducer, the train is travelling from B to A, otherwise train has changed direction. *Gating transducer B count* is incremented and P3.4 is set to 0 (next interrupt must be the falling edge of transducer B).

6 - (P0.2 = 1, P3.4 = 0) This is the falling edge interrupt from transducer B. Port 3 is modified to xxx1xxxx, enable the rising edge interrupt of transducer B. This puts interrupt control back in order if the train has changed its direction.

7 - (P0.1 = 1, P3.2 = 1). This is the interrupt from the negative half of transducer A. There is a reversal in the transducer signals; the rising edge was expected but the negative interrupt was received. The *reverse transducer A count* is incremented, and port 3 is modified to xx011011. This allows positive pulse interrupts from both transducers. *Gate sequence* is not changed so that the next interrupt might set everything back to their logical positions.

8 - This step is executed if there are errors on the interrupts. At this time the *interrupt error flag* is set. This flag is used at the "End Of Train" timeout to print a proper message to the chart recorder. Port 3 is set to xx011111, enabling all the interrupts.

Direction 2

Wheels are traversing transducer B first. If the interrupt is from P0.2, and P3.4 is set to one and step 9 is executed. Step 10 is executed which checks for possible noise and/or reverse polarity.

9 - Same as step 3 (Direction 1), except *gate transducer B count* is incremented, and port 3 is modified to xx001000.

10 - Same as step 4, except the following guidelines are used:

- * First check for an interrupt from the positive half of transducer A (P0.0). If P0.0 is one, then P3.1 is examined, to determine whether the interrupt belongs to the rising or falling edge of positive half. If P3.1 is one (rising edge) step 11 is executed, otherwise (falling edge) step 12 is executed.

- * P0.3 is examined, to determine whether the negative half of transducer B is the source of interrupt. If P0.3 is one, P3.5 is examined. P3.5, which is controlled by the software, indicates whether the interrupts from P0.3 are allowed or not. If P3.5 is one, step 13, which performs the reversal polarity logic, is executed, otherwise step 14 (errors on interrupts) is executed.

- * If all the tests mentioned fail, step 14 is executed. The only interrupts which are not checked are:

- ** Negative half of transducer A.

- ** Falling edge of transducer B.

11 - (P0.0 =1, P3.1=1) This is the rising edge interrupt from transducer A. If this is the first signal from the transducer the train is travelling from A to B, otherwise train has changed direction. *Gating transducer A count* is incremented and P3.1 is set to zero (next interrupt must be the falling edge of transducer A).

12 - (P0.0 =1, P3.1=0) This is the falling edge interrupt from transducer A. Rising edge interrupt of transducer A is enabled by setting P3.1 to one.

13 - (P0.3 =1, P3.5=1) *Reverse transducer B count* is incremented, and port 3 is modified to xx011011. This allows positive pulse interrupts from both transducers.

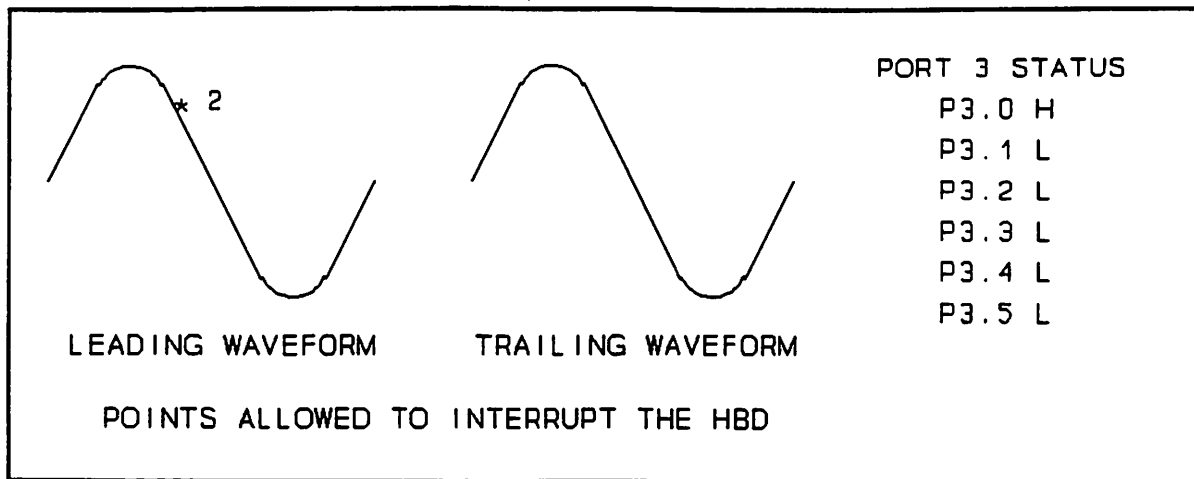
14 - (errors on interrupts) *Interrupt error flag* is set, and port 3 is set at xx111111, enabling all the interrupts.

ISR Part 2 (Gate Sequence = 2)

This section processes the trailing edge of the leading waveform (interrupt point 2). For direction 1 the interrupt must be from P0.0, while P3.1 is 0. For direction 2, the interrupt must be from P0.2, while P3.4 is 0.

Direction 1

A proper interrupt is from P0.0, otherwise an error has occurred (at this point the rising edge has been processed, and the falling edge interrupt is expected). If the interrupt is from P0.0,



P3.1 is examined. For the falling edge interrupt, P3.1 must be zero. If every thing is in proper order (P0.0 = 1, P3.0 = 1, P3.1 = 0), step 15 is executed, otherwise step 16 is executed to check for possible errors.

15 - The followings are performed during this step:

- a - *Timer 1* (the axle spacing timer) is stopped. Its value is saved for the current axle, and then re-initialize to zero for next axle. *Timer 1* holds the time interval between the current axle, and previous axle (at the current speed). Note: that for the first axle, this timer will not have valid data (its value will not be used for the car recognition).
- b - IC28(U25) heat multiplexer is directed from -6 VDC to the heat channel, to start peak hold measurement (port 5 is modified to xxx001xx, enabling the IC28(U25) and pointing the peak hold output to the CH1_PK, and CH2_PK output of IC).
- c - TB10-8 (P0.7 of digital board) is grounded, to inform the outside world of arrival of a new axle. TB10-8 is also used to turn the front panel "WHL_GATE" LCD on.
- d - Port 3 is set to xx010111, disabling transducer B interrupts, and enabling rising edge of transducer A, and negative half of transducer A.
- e - Gate sequence is set to 3, and control is passed to step 1.

16 - The *transducer interrupt error code* is set for end of train error processing. Port 3 is also modified to xx000001. The only allowed interrupt is still the falling edge of transducer A. Regardless of the error (what caused an interrupt), setting port 3 to xx000001 allows the next wheel to generate the falling interrupt.

Direction 2

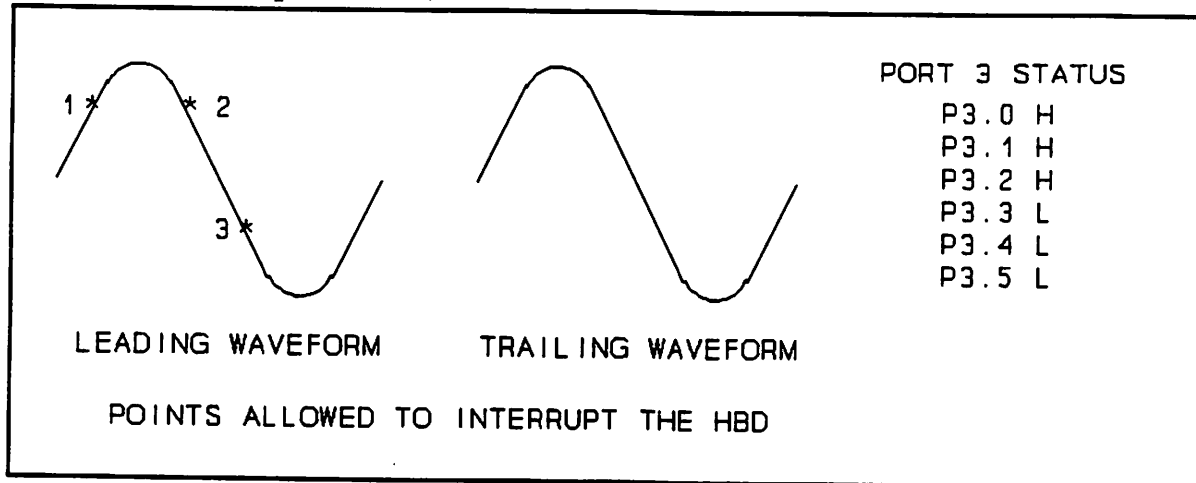
A proper interrupt is from P0.2, otherwise an error has occurred (at this point the rising edge

has been processed, and an interrupt is expected from the falling edge interrupt). If the interrupt is from P0.2, P3.4 is examined. For the falling edge interrupt, P3.4 must be 0. If every thing is proper order (P0.2 = 1, P3.3 = 1, P3.4 = 0), step 17 is executed, otherwise step 18 is executed to check for possible errors.

17 - Same as step 15. except port 3 is set to xx111010.

18 - Same as step 16, except port 3 is set to xx001000.

ISR Part 3 (Gate Sequence = 3)



This section processes the negative half of the leading waveform (interrupt point 3). This interrupt is used to verify a true sine wave from the leading transducer. The actual operations are performed by another routine which is called once every 4 milliseconds (time interrupt driven routine). This routine determines whether the current waveform is real or if it was a noise pulse. If it was a noise pulse the signal should be gone in 4 milliseconds (the code for 4 millisecond wait period is set during the rising edge interrupt of leading transducer). If it is a valid waveform the signal should still be in a verifiable form. If there is no signal an initialization is done, which resets all the interrupt controls for the rising edge interrupt of the leading waveform (gate sequence = 1). The verification routine examines P0.1 for direction 1, and P0.3 for direction 2 (negative half of leading waveform).

Direction 1

The proper sequence for this interrupt is if P0.1 interrupted the HBD software P3.2 must also be 1. The following guidelines are used to select the proper step:

* If the interrupt is from P0.1 (negative pulse of A, P0.1 = 1, P3.2 = 1) execute step 19.

* If the interrupt is NOT from transducer A (both P0.0 and P0.1 are 0), execute step 20 (error on interrupts).

* If the interrupt is from positive half of transducer A (P0.0 is one), then examine P3.1. If 3.1 is one, the interrupt is the leading edge of transducer A, execute step 21. Otherwise (P3.1 = 0), the interrupt is from the falling edge of transducer A, execute step 22.

19 - At this point, the leading edge of the trailing waveform, and the leading edge of the leading waveform are enabled (set port 3 to xx111011). The gate sequence is set to 4.

20 - The *transducer interrupt error code* is set for end of the train processing, and port 3 is set to xx010111.

21 - *Gate transducer a count* is incremented, and port 3 is set to xxxxxx0x, which enables the falling edge of the transducer A.

22 - Port 3 is set to xxxxxx1x, which enables the rising edge of transducer A.

Direction 1

The proper sequence for this interrupt is if P0.3 interrupted the HBD software P3.5 must also be one. The following guidelines are used to select the proper step:

* If the interrupt is from P0.3 (negative pulse of B, P0.3 = 1, P3.5 = 1) execute step 23.

* If the interrupt is NOT from transducer B (both P0.2 and P0.3 are 0), execute step 24 (error on interrupts).

* If the interrupt is from positive pulse of transducer B (P0.2 is one), then examine P3.4. If 3.4 is one, the interrupt is the leading edge of transducer B, execute step 25. Otherwise (P3.1 = 0), the interrupt is from the falling edge of transducer B, execute step 26.

23 - The leading edge of trailing waveform. The leading edge of leading waveform is also enabled for diagnostics. Port 3 is set to xx011111. The gate sequence is also set to 4.

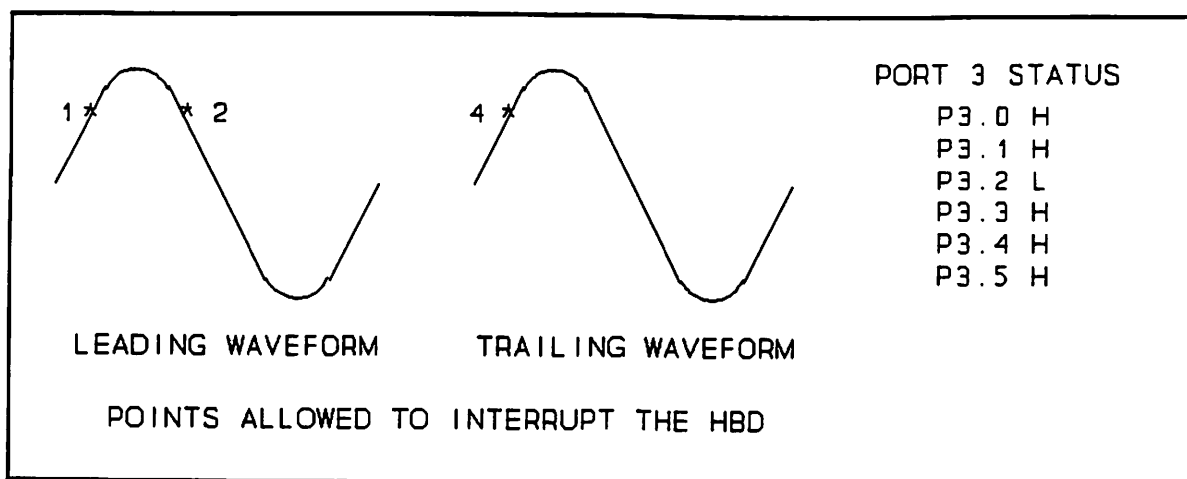
24 - The *interrupt error code* is set for end of train processing, and port 3 is set to xx111010.

25 - *Gate transducer B* count is incremented, and port 3 is set to xxx0xxxx, to enable the falling edge of transducer B.

26 - Port 3 is set to xxx1xxxx, to enable the rising edge of transducer B.

ISR Part 4 (Gate Sequence = 4)

This section processes the leading edge of the trailing waveform (interrupt point 4). For direction 1, the interrupt must be from P0.2, while P3.4 is 0. For direction 2, the interrupt must be from P0.0, while P3.1 is 0.



Direction 1

The proper interrupt should be from P0.2 (P3.3 must also be one), while P3.4 is set to 1. In this case step 27 is executed, otherwise the logic for errors/polarity reversal is executed. First the interrupts from gating transducer A are examined (in case transducer B is faulty. In the case of a faulty transducer, every four gate counts will equal one axle (the logic is described later). The negative half of transducer B is also examined for polarity reversal. In any case the following guidelines are used to determine which step to execute:

- * If interrupt is from positive half of transducer A, examine P3.1 for rising or falling edge interrupts. If P3.1 is 0 (falling edge), step 30 is executed. If P3.1 is one (rising edge), step 31 is executed.
- * If the interrupt does not belong to gating transducer A, the negative half of transducer B is examined. If P0.3 is one, step 28 is executed, which consists of polarity reversal logic. However, if P0.3 is 0, step 29, which processes errors on interrupts, is executed.
- * If the interrupt is NOT from P0.0 (positive half of the transducer A), reverse polarity is checked. If the interrupt is from P0.3 (negative pulse of transducer B), execute step 28 for reverse polarity, otherwise execute step 29 for errors on interrupts.

27 - Gate transducer B count is incremented. Port 3 is set to xx001000. The new mask disables all the interrupts, except the falling edge of trailing waveform (transducer B). The *Gate sequence* is also set to 5.

28 - (reverse polarity). The *reverse transducer B count* is incremented, and port 3 is set to xx011011. The new mask enables the rising edge of both waveforms.

29 - (errors on interrupts). The *transducer interrupt error flag* is set, and port 3 is modified to xx111011.

30 - Port 3 is modified to enable the rising edge of transducer A (xxxxxx1x).

31 - *Gate transducer A count* is incremented, and port 3 is set to enable the falling edge of transducer A (xxxxxx0x).

Direction 2

The proper interrupt should be from P0.0 (P3.0 must also be one), while P3.1 is set at one. In this case execute step 32, otherwise use the following guidelines to determine which step to execute.

* If the interrupt is from P0.2, then P3.4 is examined. If P3.4 is 0, step 35 is executed, otherwise step 36 is executed.

* If the interrupt is NOT from transducer B (P0.2), reverse polarity is checked. If the interrupt is from P0.1 (negative pulse of transducer A), execute step 33 for reverse polarity, otherwise execute step 34 for errors on interrupts.

32 - The trailing edge of the trailing waveform is enabled, by setting port 3 to xx000001. The new mask disables all the interrupts, except the falling edge of transducer A. The *gate transducer A count* is incremented, and The *Gate sequence* is also set to 5.

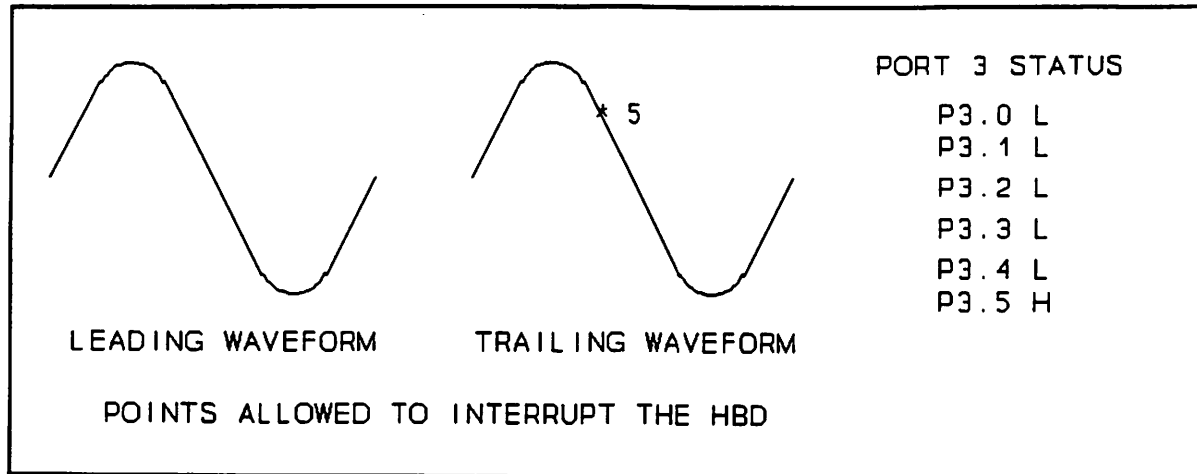
33 - (reverse polarity). The *reverse transducer A count* is incremented, and port 3 is set to xx011011.

34 - (errors on interrupts). The *transducer interrupt error flag* is set, and port 3 is set to xx011111.

35 - Port 3 is modified to enable the rising edge of transducer B (xxx1xxxx).

36 - The *gate transducer B count* is incremented, and port 3 is set to enable the falling edge of transducer B (xxx0xxxx).

ISR Part 5 (Gate Sequence = 5)



This section processes the trailing edge of the trailing waveform (interrupt point 5). For direction 1, the interrupt must be from P0.2, while P3.4 is one. For direction 2, the interrupt must be from P0.0, while P3.1 is one. This interrupt indicates wheel departure.

Direction 1

The proper interrupt should be from P0.2 (P3.3 must also be one), while P3.4 is set to 0. In this case step 37 is executed, otherwise step 38 is executed for errors.

37 - This step concludes the interrupts for the current wheel. First *timer 2* (train speed timer) is stopped, its value is used to calculate current speed of train (it is also used for car recognition). At this time the optical shutters are closed, by clearing P2.6 (digital board), and TB10-8 (P0.7 of digital board) is set to 12 VDC, indicating departure of wheel. TB10-8 is used to turn the front panel "WHL_GATE" LCD off. The scanner heat signals are then processed (for a detailed explanation of how the scanner signals are processed, refer to "SCANNER HEAT" section of document). After storing channel 1 and 2 heat values (channel 3 and 4 in case of Hot Wheel detectors), the auxiliary port (digital board port 0), is examined for any alarms. P0 is then cleared. Note: The external alarm inputs are turned off, so that the filtering caps have time to charge before internal alarms are cleared. At this point the number of axles is incremented. Finally port 3 is set to xx011111, enabling all interrupts for next wheel (gate sequence is also set to 1).

38 - *Transducer interrupt error flag* is set for end of train processing. Port 3 is set to xx001000 (an interrupt from transducer B is needed to finish the current wheel).

Direction 2

The proper interrupt should be from P0.0 (P3.0 must also be one), while P3.1 is set to 0. In this case step 39 is executed, otherwise step 40 is executed for errors.

39 - Same as step 37.

40 - *Transducer interrupt error flag* is set for end of train processing. Port 3 is set to xx000001.

End of Train Processing

Data Communications Processor Software

The Harmon Data Communications Processor (DCP) is an option family for the Harmon Hot Box Detector (HBD) System providing on site archival storage of train passage information and data communications between the HBD and a local or remote operator. This family of add on communications systems comes in three varieties: the DCP-2, the DCP-2+, and the DCP-3. Information contained in this section is written to be used with any of the DCP units. Any differences between the three types of DCPs will be addressed at specific points in the text. The operation and functionality is exactly the same for all three DCPs; the only differences are in the system hardware.

Operating Parameters

The following is a summary listing of the general operating parameters of the DCP:

	<u>DCP-2</u>	<u>DCP-2+</u>	<u>DCP-3</u>
Maximum number of trains:	64	180	64
Maximum number of defect trains:	5	10	5
Maximum train sequence number:	9999	9999	9999
Maximum number of axles:	18000	54000	18000
Maximum number of defect axles:	2000	6000	2000

Heat value display: Selectable -

degrees Celsius
degrees Fahrenheit
Millimeters

Milepost maximum:	999.9	miles
Axle timeout:	54	Minutes
HBD inquiry retries:	3	times
Minimum axles per train:	4	axles

Alarm level ranges

	<u>MIN</u>	<u>MAX</u>
Maximum number of alarms	5	12
Hot bearing low limit	23	70
Hot bearing high limit	70	112
Car side slope adjust	0.68	2.36
Car side limit	23	70
Hot wheel limit	200	600

Memory

Program code for the DCP is stored in 64K bytes of EPROM memory. In addition, 256K bytes of battery backed static RAM (768K on the DCP-2+) are used to store program variables and archival train data. The battery backed static RAM may be cleared by removing jumper W5 on the DCP board (jumper ?? on the DCP II) for 15 seconds.

Train and axle data are stored in two separate memory buffers. One is used for the Standard train memory and the other for the Defect train memory.

Standard train memory is used to store train and axle data for all trains and accepts data for test trains as well as real trains. Defect trains are stored in the Standard memory along with those not containing defects. This buffer has a 64 train or 20,000 axle capacity (180 trains and 54,000 axles for the DCP-2+). What data will be retained depends upon memory usage - a 65th train will overwrite the first one even though there may not yet be 20,000 axles stored. Similarly, the 20,001st axle will overwrite the first one even if there are not yet 64 trains in memory.

Train and axle data stored in the Standard train memory is retained even when power is disrupted to the HBD and/or the DCP.

Train and axle data for trains with defects are copied to the Defect train memory. The purpose of this memory is to aid in maintaining a record of defective train passages. To make for more accurate and clear defect train records, test trains will not be stored in the Defect memory.

The data that is contained in the Defect memory has been copied from the Standard memory. Therefore, information contained in the Defect memory may be accessed from either section until it is overwritten by subsequent train passages. If the data is over-written in one area, it will still be contained in the other until that area is also over-written. This is desirable for locations with high numbers of train passages in a short period of time. In this situation, data in the Standard memory tends to be over-written relatively quickly. The Defect buffer allows the defect train information to be retained for a longer period of time.

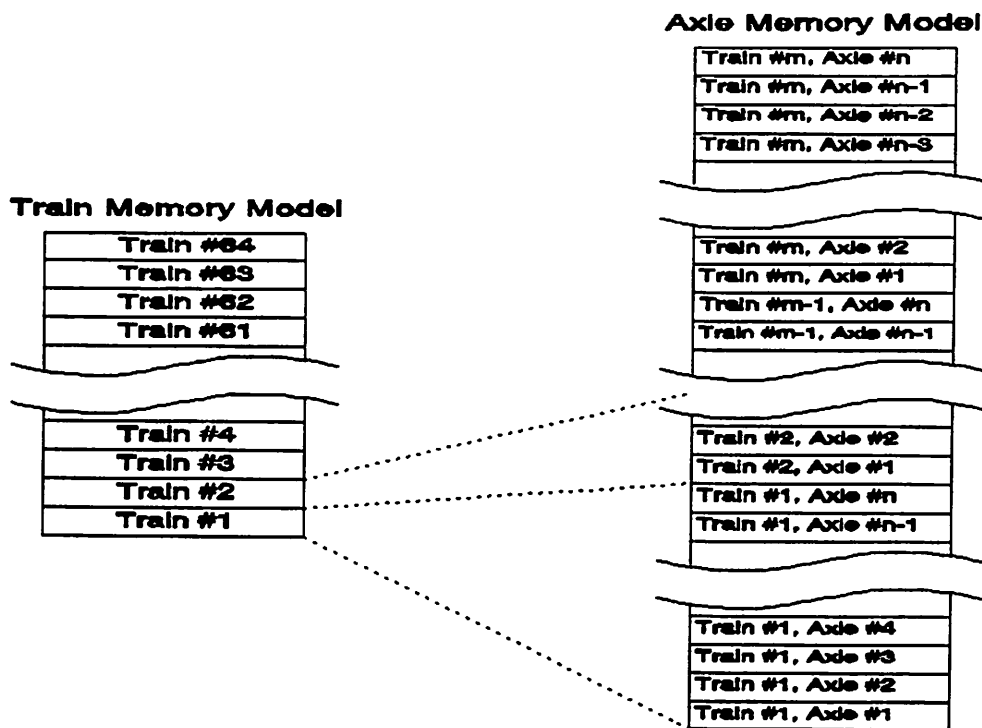


Figure X.14

Each memory buffer is organized as a pair of circular queues; one is for general train information and the other for axle data. When transmitted from the HBD, general data about the train is placed in the first storage area in the train queue. As the axle data is received, it is placed in the axle data queue. The next train will be placed in the queue behind the first train and its axle information will be placed in the axle data queue behind the axle data for the first train. Figure X.1 illustrates how this storage structure works using the DCP-3 parameters.

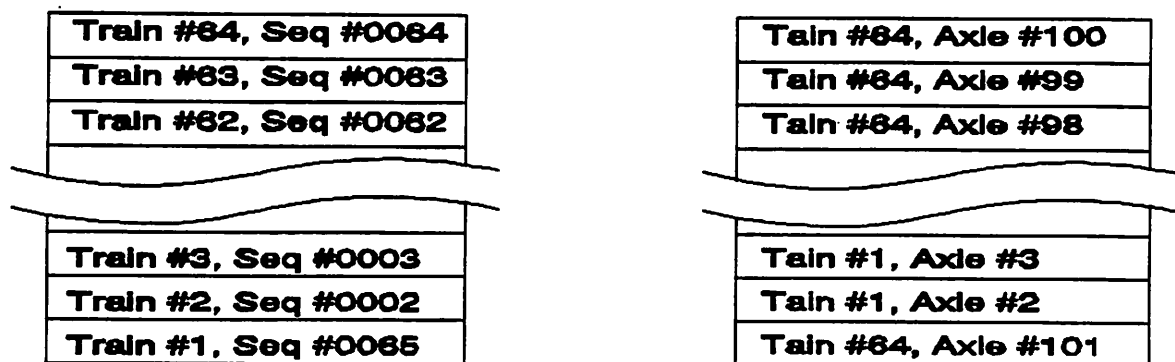


Figure X.15

When either of the queues is completely filled, the next data item to be stored in that queue is placed in the first queue position and the previous information stored in that location is erased. This results in a first-in-first-out storage system, where the newest set of train data overwrites the oldest set of data. The software maintains specific pointers to be able to locate the most recent train and axle data in the queues. Figure X.2 shows how this situation would work when the axle data queue becomes filled.

Powerup

When the DCP powers up several actions take place before the software is ready to perform its required functions: memory must be initialized and/or verified, the communications ports must be configured, and individual program tasks initiated. As the DCP has a multi-tasking program kernel, it is capable of performing multiple operations simultaneously. Each of these tasks must, therefore, be set up and configured.

Because the RAM memory has a battery backup feature, it is necessary to verify the validity of the memory every time the DCP is powered up. A specific location in RAM is checked against values stored in the ROM. If this checksum is valid it is assumed the battery backup feature has been active and successful. If not then the memory is initialized. Some areas of memory are initialized every time the DCP initializes. Those visible to the user are the site name and mile post number. The site name is set with the Name command in the Maintenance Mode; the mile post information is received from the HBD/HWD at the end of train passage.

Regardless of the outcome of the powerup checksum test above, the train data memory segment is also tested for validity. When train data is stored in memory, a checksum is computed on the data and stored along with the train data. At powerup, each train stored is checked against these checksums. If the data for any train is corrupt, then that entire train is deleted from memory. In addition to the memory verification, the software loads and initializes all tasks into the multi-tasker. The following is a list of all tasks loaded and a brief description of each:

HBDTask: Waits for messages from the HBD/HWD.

StatusTask: Monitors the external status lines for change.

WatchTask: Monitors a watchdog timer and prevents the multi-tasker from resetting the system should no task reset the timer within a specified period.

LocalTask: Monitors the Local Port for user commands.

RemoteTask: Monitors the Remote Port for user activity via a modem attached to this port. A Modem attached to this port will be initialized when the task begins operation.

AuxTask: Monitors the Auxiliary Port for user activity via a modem attached to this port. A Modem attached to this port will be initialized when the task begins operation.

After the memory check, the multi-tasking kernel is started and allows all tasks to operate. Each task is given a small amount of processor time to complete a portion of its assignment. Then the next task in line is allowed to operate for a while. This rotation through the tasks takes place very quickly and is generally unnoticeable to the user. However, the DCP is then able to accomplish many different operations at the same time. For example, the DCP could be receiving train data from the HBD/HWD while at the same time be communicating with a person connected through a local printer or terminal and also be receiving instructions via the modem communications channel. At no time would any of the three connections know the others were present, nor would they be affected.

Signon

When a terminal is connected to the LOCAL port, a signon message is printed whenever the DCP is first reset. This confirms that the DCP has gone through a power-on sequence. The program maintains an internal check to keep track of the validity of data stored in memory. Should this value become corrupt, some settings, such as status point names and the site name, will be reset. If the value is correct, no user settings are initialized. In either case, all train and axle data is checked for data integrity and deleted if not valid.

A signon message is also printed automatically when calling in to the REMOTE port. The DCP does not reset, initialize, or do an integrity check in this case. It merely confirms that a connection has been made.

For double track systems accessed remotely, there is one additional operation required before the signon message is displayed. In this configuration, the DCPs can be set up to share one modem. The Remote Port cables are attached to a specialized multiple port junction box and one cable comes from the master port and attaches to the modem. The Ring Indicate line on each of the ports in the junction box has been tied together. Up to three DCPs can be set up to share one modem in this fashion.

When these DCPs are accessed remotely, they must be informed which system is desired. To accomplish this, the caller must press the <CONTROL> key simultaneously with the <G> key followed by the HBD detector number for the desired system (i.e. <1> or <2>). The requested DCP will then respond with the signon message.

The signon message includes the time and date as stored on the DCP itself. The DCP can operate as a stand-alone device (except that no train data will be captured) as it does not require the HBD/HWD to maintain the time and date. Because it has its own clock and calendar function, it is possible for the DCP to become slightly out of sync with the HBD/HWD. To compensate for this situation, the DCP time and date are synchronized to the HBD/HWD after every train passage.

The signon message also contains the version of the firmware running in the DCP. This version should be referred to whenever contacting Harmon Electronics, Inc. with questions regarding the program.

User Interface

The current operator interface has been implemented as a command line entry system. This has minimized wasted terminal paper by eliminating the repetitious reprinting seen in the older menu driven systems. Once familiar with the system, the commands are intuitive enough to enable rapid control of the system functions.

To provide a more functional organization to the commands, the concept of 'modes' has been implemented. Each of the DCP commands has been placed into one of three modes, based on the general function associated with each mode. The three modes are 'Display', 'Alarm', and 'Maintenance.'

In addition, 'Help' printouts are available for those not completely familiar with the system. To access the 'Help' screen, type a <?> at the command prompt followed by pressing <RETURN>. A short description of each command and the use of any options or parameters will be displayed.

Throughout the DCP program, if a particular piece of information such as train direction, outside temperature, etc., is unknown at the time of the request, asterisks (*) are printed in place of the value. Generally, this occurs because available functions (such as the ambient temperature probes) have not been incorporated into the system. A second explanation is that the communication between the DCP program and the HBD/HWD is not complete. Another possibility is that a reset or the arrival of a train interrupted processing in the HBD/HWD.

Command Line Entry

The DCP utilizes three operational modes in the user interface: Display Mode, Maintenance Mode, and Alarm Mode. Each has a particular function and contains specific commands that are unique to that functional group.

A single letter designation followed by the '>' symbol is used as the command line prompt with the letter indicating the current mode. The designator for the three modes are as follows:

D> for Display Mode
M> for Maintenance Mode
A> for Alarm Mode

When the command prompt is present, the DCP is ready to accept commands. To change from one mode to the other, type <M>, the designator for the new mode (<D>, <M>, or <A>), and then press the <RETURN> key. As an example, the entry to go from Display Mode to Alarm Mode would look like this:

D> <M> <A> <RETURN>

If only <M> <RETURN> is entered, the user will then be prompted to enter the new mode desired.

Access to the Alarm and Maintenance Modes may be dependent upon password verification if the system is configured to require a password.

A help screen may be accessed by typing <?> <RETURN>. This will display all of the commands available for the current mode, along with a brief description of each command function.

The command line entry system entails the input of the command letter followed by <RETURN>. Limited line editing may be accomplished by using the backspace, delete, or rub-out key to backup over previously entered characters.

Some commands allow a specification character or value to be entered on the same line as a command letter. The Mode selection discussed above is a good example. Other commands will either perform the desired task immediately or prompt the user for the necessary information. All commands will be explained in a later section.

Commands which generate long outputs may be aborted by using <ESC>. When the <ESC> key is used, the function is stopped and the message '*** break ***' is displayed at the point in the display where the function aborted. A command cursor will then appear telling the user that the DCP is ready for the next command.

Display Mode

This is the mode used most frequently and provides the capability to display listings and reports. The following is a list of the commands available while working in the Display Mode:

- <L> Provides a listing of all trains stored in the standard memory.
- <L> <D> Provides a listing of all defect trains stored in the defect memory.
- <D> <#> Displays a complete data listing for the train number specified including data on each axle. If no number is specified, the most recent train will be displayed.
- <R> <#> Displays a report for the train number specified. If no number is specified, the most recent train data will be displayed. This listing does not include axle data information.
- <A> <#> Displays a full train listing and alarm axle data for the train number specified. If no number is specified, the most recent train data will be displayed.
- <T> <#> Initiates a train test where '#' is the desired train speed: 1 = SLOW (approx. 30 MPH), 2 = MEDIUM (approx. 60 MPH), and 3 = FAST (approx. 130 MPH).
- <S> Displays the current site status points.

- <I> Displays the site information.
- <ESC> Will stop a listing and return to Display mode command prompt.
- <M> <m> Change mode, where 'm' is D for display mode, A is for alarm mode, or M is for maintenance mode.
- <Q> Disconnect a remote user from DCP.

Following are examples of each listing/display offered by the DCP Display Mode and how to read the data.

***** <L>ist command *****

The List command displays a listing of all trains in the standard memory buffer. An example of a train listing is shown below. The layout for the display begins with a short header giving the railroad name, milepost, site name, and firmware version information. Trains are then listed in chronological order with the most recent train being at the top of the list. What follows is a brief explanation of each column in the the listing and where the information is obtained.

Train Number	Gives the number in the DCP corresponding to the location in the memory buffer discussed above. This number is also used when utilizing the D, R, and A commands to identify the train desired. A 'T' appearing immediately after the train number indicates a test train.
Sequence Number	This number uniquely identifies the train in the DCP and ranges from 0001 to 9999. Once the 9999th train passes, the sequence is reset to 0001. Using this number will provide the user an indication as to the number of passages occurring withing a given time period.
Direction	Show in what direction the train was proceeding.
Speed	Represents the speed the train was travelling when it exited the detector.
Axle Count	Provides the number of axles processed by the DCP.
Car Count	Indicates the number of cars as reported by the HBD.
Train Length	Calculated from raw data recieved from the HBD.
Defect Count	Represents the number of defects processed by the DCP.
Integrity Failures	Represents the number of integrity failures processed by the DCP.
Warning Count	Represents the number of warnings processed by the DCP.
Time	Represents the time at which the detector timed out and sent the end of train data message.
Date	Represents the date of train passage.

D>L

Railroad Name MILEPOST: 1234.5

**** HBD/HWD v3.8 DCPx v3.1

--ALL TRAINS--

TRN #	SEQ #	TRN DIR	TRN SPD	AXLE CNT	CAR CNT	TRN LEN	DEFECT CNT	INTEGRITY FAILURES	WARNING CNT	TIME	DATE
3	00003	N	63	112	27	1060	3	0	0	7:04	90-09-16
2	00002	N	18	22	7	235	0	0	0	5:33	90-09-16
1T	00001	N	47	20	7	233	1	1	3	5:29	90-09-16

Note, if the DCP has not recieved information from the HBD/HWD since the last powerup, the HBD/HWD version and the milepost number will be displayed as 0.0. This information will be updated after the next train passes the detector. In addition, if the site name has not been set, '*****' will be displayed. For more information on setting the site name see the N command under Maintenance Mode.

***** <L>ist <D>efects command *****

The List Defect command displays a listing of all trains currently in the defect train memory buffer. The format is identical to the List command above except the train numbers will range from 65 to 69 (181 to 190 on the DCP II+). The sequence number will allow the user to reference the train cronologically with respect to the trains in the <L> listing.

D>LD

TRN #	SEQ #	TRN DIR	TRN SPD	AXLE CNT	CAR CNT	TRN LEN	DEFECT CNT	INTEGRITY FAILURES	WARNING CNT	TIME	DATE
65	00003	N	63	112	27	1060	3	0	0	7:04	90-09-16

***** <R>eport, <D>ump and <A>larm List command *****

The Report, Dump, and Alarm commands are similar in their contents. The Report command provides a detailed account of the train specified in the command line (i.e. R4 will report on train four in the train list). Information provided in the output header includes the following:

Train Number	Number in DCP memory
Sequence Number	Identifier number
Railroad Name	Name of railroad as sent by HBD
Milepost	Milepost setting as sent by HBD at the end of train passage.
HBD Version	Version of HBD firmware. Sent after train passage.
DCP Version	Internal software version number for DCP.
Inside/Outside Temp	Sent from HBD.
Defect Count	Number of defects processed by the DCP.
Direction	Sent from HBD.
Axle Count	Number of axles as seen by HBD. Sent from HBD.
Car Count	Number of cars as seen by HBD. Sent from HBD.

Speed In	Represents the speed of the train as axle number four passed the detector.
Speed Out	Speed of the train as it left the detector.
Integrity	Specifies if the HBD passes its integrity tests.
Length	Length of train as sent by HBD.
Arrival Time	Time DCP recieved start of train message from HBD.
Departure Time	Time DCP recieved end of train message from HBD.

If the detector radio has been muted using the HM command (Maintenance Mode), an additional message is added at the end of the header.

After the header, any alarms for the train will be printed. No more than the maximum number of alarms will be output. (See Alarm Mode command C for more information on the maximum number of alarms allowed. An alarm, or defect, is one that the HBD/HWD determines to be a defect in the train itself, such as a hot bearing or wheel. The last line of the alarms section give the front panel dip switch setting as a two digit hexadecimal number.

Following the alarm section will be an explanation for any system integrity failures. An integrity failure is a condition in the HBD/HWD that might cause it to erroneously misinterpret or incorrectly identify defects of the train.

The next section displays a list of all system warnings. A warning is another type of failure of the HBD/HWD but one that does not necessarily prevent it from performing its function. Warnings tend to be for maintenance and informational purposes.

The last section of the output is a listing of the current alarm levels for the system.

When the Dump command is issued, the display is the same as the Report command with the addition of axle data information listed immediately after the warning section. The axle listing contains the following data in columnar format:

Car Number	The car count from the head of train based on data in the axle message specifying this as the first axle of a car.
Axle Number	The axle count from the head of train as received from the HBD.
Axle Spacing	The number of feet between axles.
Bearing Heats	Channel 1 and Channel 2 heat values. They are displayed in the units (millimeters, Farenheit, or Celcius) as set in the Maintainence Mode with the Y command.
Wheel Heats	Channel 3 and Channel 4 heat values.
Alarms	If any axle specific alarms or warnings are present they will be specified in this area.

The Alarm list command is identical to the Dump command with the exception that only a certain range of axles is displayed instead of the entire list. The axles displayed include the ten axles previous to any alarm axle and the ten after the alarm. If there are more than one alarm and they are sufficiently far apart, the axle display would appear to have gaps in the axle listing.

This is intentional as only the desired axles are shown.

For any of these three commands, the user may specify a train number to indicate a particular train desired. If no train number is input, the last train recorded will be displayed.

The following listing is for a Dump command but also provides the information contained in the Report and Alarm commands.

```
D>D
--TRAIN #1, SEQ. #0--
Railroad Name      DEFECTS:          13  HBD INTEGRITY:    FAIL
MILEPOST:          1234.5  DIRECTION:      W  TRAIN LENGTH:  2559 FT
**** HBD/HWD v3.8 DCPx v3.1  AXLE COUNT:    172  CURRENT:  2:07 90-08-20
OUTSIDE TEMPERATURE:  71 C  APPROX. CARS:    42  ARRIVE:   1:25 90-08-20
INSIDE TEMPERATURE:   ***  SPEED IN/OUT    63/63  DEPART:   1:26 90-08-20
*** HBD Radio muted ***
```

--ALARMS--

```
Hot bearing at axle 21, car 5 on the North rail  20.0 mm Absolute
Hot Wheel from axle 21, car 5 to axle 24 on the North rail
Hot bearing at axle 32, car 7 on the North rail  25.0 mm Absolute
Dragging equipment near axle 84, car 20
High load near axle 87, car 23
Hot bearing at axle 88, car 24 on the South rail  17.0 mm Differential
Wide load near axle 91, car 25 on the South rail
Wide load near axle 95, car 26 on the North rail
Loose wheel near axle 102, car 28
Hot bearing at axle 172, car 45 on the North rail  17.2 mm Car side
Front Panel Switches: BF FF
```

--INTEGRITY FAILURES--

```
Channel 4 protective shutter stuck closed
```

--WARNINGS--

```
Too many alarms
HBD power-on reset since last train
```

--AXLES--

CAR #	AXLE #	AXLE SPACING	BEARING ch1	BEARING ch2	WHEEL ch1	WHEEL ch2	ALARMS
							-----Millimeters
1	1	0.5	4.0	3.4	3.8	4.2	
	2	6.8	3.1	3.8	3.4	3.8	
	3	6.8	3.1	3.1	3.6	3.8	
	4	31.3	3.4	4.0	3.6	3.8	
	5	6.8	3.8	4.2	3.6	4.2	
	6	6.8	3.8	3.8	3.6	4.6	
2	7	16.0	4.0	4.2	4.4	5.4	
	8	6.8	3.2	3.6	3.6	4.6	
	9	6.8	3.1	3.2	3.6	5.0	
	10	31.3	3.8	2.6	3.8	4.6	
	11	6.8	3.1	3.4	3.8	5.0	
	12	6.8	3.2	3.8	3.6	4.6	
3	13	16.0	6.6	9.6	3.8	4.6	
	14	8.6	8.8	9.4	4.0	5.0	
	15	30.4	7.2	8.6	3.6	4.6	
	16	8.5	8.6	8.4	3.8	5.2	
4	17	14.9	5.8	8.0	3.8	4.2	

	18	4.9	7.8	6.6	3.6	4.4		
	19	35.9	6.4	6.4	4.2	3.8		
	20	4.9	7.0	6.4	4.4	3.8		
5	21	11.3	8.2	20.0	5.0	23.8	AA	HW
	22	4.9	5.8	16.2	5.0	23.4	HW	
	23	35.9	5.0	15.2	5.0	24.2	HW	
	24	4.9	9.4	15.8	5.0	24.2	HW	
6	25	11.3	5.6	5.0	3.6	4.4		
	26	4.9	7.0	5.4	4.4	4.0		
	27	36.0	6.2	5.8	4.0	4.4		
	28	5.0	8.6	6.8	3.6	4.2		
7	29	11.3	14.4	14.4	3.8	4.2		
	30	5.0	14.4	14.4	4.4	4.4		
	31	36.0	14.4	14.4	4.0	4.4		
	32	5.0	14.4	25.0	3.6	4.4	AA	
8	33	11.4	5.0	5.2	4.0	4.4		
	34	5.0	7.6	8.8	4.4	3.8		
	35	36.3	5.8	6.6	3.8	4.4		
	36	4.9	7.4	5.8	3.6	4.2		
9	37	11.4	5.0	4.8	3.8	4.2		
	38	5.0	6.8	6.2	3.8	4.2		
	39	36.5	6.4	8.6	3.8	4.2		
	40	5.0	6.6	4.0	3.8	4.2		
10	41	11.3	6.4	7.0	3.8	4.2		
	42	4.9	7.0	7.0	3.8	4.2		
	43	36.5	7.0	6.0	3.8	4.2		
	44	4.9	8.4	7.0	3.8	4.2		
11	45	11.3	7.0	5.4	4.4	4.4		
	46	5.0	7.0	7.0	3.8	4.2		
	47	36.5	6.0	6.0	4.4	3.8		
	48	5.0	9.4	8.8	4.2	3.8		
12	49	11.3	7.8	6.0	3.8	4.2		
	50	5.0	7.6	9.8	4.4	3.8		
	51	36.4	7.6	4.8	4.2	4.2		
	52	5.0	7.0	7.8	4.4	3.8		
13	53	11.3	4.0	4.8	4.8	4.6		
	54	5.0	6.8	5.0	4.8	4.6		
	55	36.3	4.0	4.8	4.8	4.6		
	56	4.9	5.2	5.0	4.8	4.2		
14	57	11.3	4.4	5.0	3.8	4.2		
	58	4.9	5.4	5.6	4.0	4.4		
	59	35.9	5.6	5.0	3.6	4.4		
	60	4.9	5.4	5.6	3.8	4.2		
15	61	11.3	4.8	5.0	4.8	5.2		
	62	4.9	5.6	5.0	4.8	5.2		
	63	35.9	5.4	4.2	3.8	4.2		
	64	4.9	5.6	4.2	3.8	4.2		
16	65	11.3	3.1	3.1	3.8	4.2		
	66	4.9	3.1	3.4	3.8	4.2		
	67	35.9	3.6	3.6	3.8	4.2		
	68	4.9	2.6	2.6	3.8	4.2		

17	69	11.3	5.8	5.4	3.8	4.2	
	70	4.9	6.0	5.4	3.8	4.2	
	71	35.9	4.8	4.8	3.8	4.2	
	72	4.9	6.6	4.8	3.8	4.2	
18	73	11.3	5.0	9.0	4.8	4.8	
	74	4.9	6.6	6.6	4.8	5.2	
	75	35.9	5.4	5.6	2.0	4.2	
	76	4.9	6.0	6.8	3.8	4.2	
19	77	11.3	4.0	4.0	3.1	3.8	
	78	4.9	5.8	7.0	3.8	3.8	
	79	35.9	5.0	6.4	3.1	3.8	
	80	4.9	6.0	6.8	3.2	4.2	
20	81	11.3	7.6	7.6	4.2	4.2	
	82	4.9	10.6	11.0	4.2	4.2	
	83	35.9	7.2	5.6	3.8	4.0	
	84	4.9	8.8	6.6	4.0	4.4	D
21	85	11.3	8.0	7.6	4.0	4.4	
22	86	35.8	6.2	6.0	4.6	3.8	
23	87	11.5	8.0	7.6	3.6	4.2	H
24	88	35.8	17.0	4.0	3.4	4.2	DA
25	89	20.4	6.2	5.6	3.8	3.4	
	90	4.9	8.8	5.2	4.6	4.2	
	91	35.8	4.0	5.0	4.4	3.8	C
	92	4.9	4.8	5.4	3.6	4.2	
26	93	11.3	4.4	4.4	3.8	4.2	
	94	4.9	5.6	5.6	3.8	4.2	
	95	35.9	4.2	4.2	3.8	4.2	C
	96	4.9	5.0	5.0	3.8	4.2	
27	97	11.3	5.0	4.8	3.6	5.2	
	98	4.9	7.8	6.0	3.6	5.2	
	99	35.9	6.0	5.0	3.6	4.8	
	100	4.9	6.0	6.2	3.6	4.6	
28	101	11.3	6.0	5.8	3.6	4.2	
	102	4.9	5.0	8.8	3.8	4.2	L
	103	35.9	6.6	5.0	3.6	4.2	
	104	4.9	7.2	8.0	4.2	4.2	
29	105	11.3	5.6	4.8	3.8	4.2	
	106	4.9	5.4	5.4	3.8	4.2	
	107	35.9	4.8	5.0	3.8	4.2	
	108	4.9	5.2	6.2	3.8	4.2	
30	109	11.3	8.6	8.8	7.4	7.2	
	110	4.9	9.0	11.0	6.2	7.2	
	111	35.9	5.8	6.6	5.8	6.2	
	112	4.9	6.8	9.8	5.8	7.2	
31	113	11.3	7.6	7.6	3.8	4.2	
	114	4.9	7.8	11.0	3.8	4.2	
	115	35.9	6.6	5.6	3.8	4.2	
	116	4.9	9.0	10.6	3.8	4.2	

32	117	11.2	6.6	6.2	3.8	4.2
	118	4.9	8.0	6.0	3.8	4.2
	119	35.9	6.0	5.8	3.8	4.2
33	120	4.9	8.2	8.2	3.8	4.2
	121	11.3	3.4	2.2	2.0	2.4
	122	4.9	3.4	2.4	3.1	3.4
34	123	35.9	2.6	2.2	3.1	2.4
	124	4.9	2.6	3.1	3.1	5.2
35	125	11.3	9.2	8.6	3.8	4.2
	126	4.9	9.4	8.6	4.2	4.2
	127	35.9	7.8	8.6	4.2	4.2
36	128	4.9	8.2	9.2	4.2	4.2
	129	11.3	5.4	5.0	3.8	4.2
	130	4.9	6.6	6.6	3.8	4.2
37	131	35.9	4.8	4.8	3.8	4.2
	132	4.9	7.2	8.6	3.8	4.2
	133	11.3	6.4	5.8	4.2	4.4
38	134	4.9	7.8	6.2	4.0	4.4
	135	35.9	5.2	5.2	4.0	4.4
	136	4.9	7.0	5.2	4.0	4.2
39	137	11.3	5.2	6.0	3.8	4.2
	138	4.9	7.0	6.6	4.0	4.2
	139	35.9	6.0	5.4	4.2	4.2
40	140	4.9	7.0	7.8	4.0	4.2
	141	11.3	7.4	6.0	3.8	4.2
	142	4.9	9.4	6.0	3.8	4.2
41	143	35.9	7.0	5.4	3.8	4.2
	144	4.9	9.6	13.4	3.8	4.2
	145	11.3	10.0	8.8	4.8	4.2
42	146	4.9	10.8	10.6	4.8	4.4
	147	35.9	7.0	6.2	4.8	4.2
	148	4.9	9.4	8.8	4.8	4.2
43	149	11.3	7.4	6.0	3.8	4.2
	150	4.9	9.4	6.0	3.8	4.2
	151	35.9	7.0	5.4	3.8	4.2
44	152	4.9	6.8	13.4	3.8	4.2
	153	11.3	7.6	7.0	5.8	6.2
	154	4.9	9.4	12.0	5.8	5.2
45	155	35.9	6.6	4.8	4.8	6.2
	156	4.9	7.0	6.8	4.8	6.2
	157	11.2	8.6	6.8	4.8	4.2
46	158	4.9	9.8	9.8	4.8	4.4
	159	35.9	8.2	5.2	4.8	4.2
	160	4.9	9.4	9.8	4.8	4.2
47	161	11.3	6.0	5.6	3.8	5.2
	162	4.9	7.8	8.0	3.8	5.2
	163	35.9	5.8	5.0	3.8	5.2
48	164	4.9	8.8	8.8	3.8	5.2
	165	11.3	8.8	8.0	4.4	4.4
	166	4.9	9.0	10.0	4.0	4.4
	167	35.9	6.0	4.2	4.4	4.2

	168	4.9	6.6	8.6	4.4	4.2	
45	169	11.3	5.2	6.0	3.6	3.8	
	170	4.9	3.4	6.0	3.6	4.6	
	171	35.9	5.6	5.4	3.6	4.2	
	172	4.9	6.2	17.2	4.2	5.2	CA

--HBD/HWD current alarm levels--Current--

Hot bearing low limit	9.0
Hot bearing high limit	18.0
Car side slope adjust	1.33
Car side low limit	8.0
Hot wheel limit	12.2
Maximum number of alarms	7

The codes for the axle alarms are as follows:

- AA = Hot Bearing (Absolute)
- CA = Hot Bearing (Car side)
- DA = Hot Bearing (Differential)
- HW = Hot Wheel
- C = Wide Load
- D = Dragging Equipment
- H = High Load
- L = Loose Wheel

******* <T>est <#> command *******

This command tells the HBD to start a functional self-test train. After the HBD has received the command, the command cursor will return to the screen and the user can use any of the available DCP functions while the data is being collected by the DCP. Note that if a <L>ist command is entered, the test train that is being run will not appear in the list until the HBD has timed out and all of the data has been sent to the DCP. The number on the test train is optional and indicates what speed of test train is to run. Possible speeds for the test train are: Fast (120 mph), Medium (63 mph), and Slow (31 mph).

******* <S>ite Status command *******

This command provides the user with a short list of the reporting sites and the status (on or off) of each. When this command is issued, the DCP immediately reads the value on each input to the Site Status Port.

The listing header displays the railroad name, date and time of report, milepost, HBD/HWD and DCP software version. After the header is displayed the number, name, and status of each site point is printed. For more information see the Site Status section below.

```

D>S
--SITE STATUS--
Railroad Name
MILEPOST:      1234.5
Rn   HBD/HWD v3.8 DCPx v3.1
--STATUS--
1  Status point 1   is OFF      2  Status point 2   is OFF
3  Status point 3   is OFF      4  Status point 4   is OFF
5  Status point 5   is OFF      6  Status point 6   is OFF
7  Status point 7   is OFF      8  Status point 8   is OFF

```

***** <I>nformation command *****

This command provides the user with a short list of site information including the location of the site as well as the version of hardware and software being utilized. When this command is issued, a message is sent to the HBD requesting the status of the HBD. If no response is recieved, the DCP will output an additional message stating that communication with the HBD is out and the values printed may not reflect current settings.

```

D>I
Detector version:    3.8
Detector type:       Hot Bearing/Wheel Detector
DCPx version:        3.1
Railroad name:       Rn
Site name:           Railroad Name
Milepost:            1234.5
*** HBD Radio muted ***
*** HBD Disabled ***
Heat values are displayed in millimeters
Current time and date is 13:52:52 Sep 26, 1991

```

***** <ESC>ape command *****

This command allows the user to stop a listing and return to the command cursor. A break message will occur where the <ESC> command was given to show that the listing is not complete.

***** <Q>uit command *****

This command tells the DCP to hang up the modem and place the DCP in the Display Mode. If a user is connected to the Local Port, then the only apparrent action is a return to the Display Mode.

Alarm Mode

This mode allows the user to view and modify parameters for the train alarm values. Access to this mode can be prevented by setting a user password as found in the Maintenance Mode section. The following is a list of the commands available while working in the Alarm

A><A><1><0><RETURN>

Should the user enter only the command without parameters, the DCP will display the current parameter level, the minimum and maximum levels allowed, and then request the new parameter level.

A>A

Current Maximum number of alarms is: 5

Minimum is: 5

Maximum is: 12

Enter new value:

When a parameter is changed, the change is immediately sent to the HBD and confirmed. If the DCP is unable to change the value a message is printed indicating no changes were made.

Maintenance Mode

This mode is where the housekeeping and system utilities are performed. As with the Alarm Mode, access to this mode can be prevented by setting a user password. More information on password protection will be found in the command description of this section.

The following is a list of the commands available while working in the Maintenance Mode:

	Reboots HBD
<C>	Initiates DCP Self-test
<D>	Allows the user to view the time and date with the option to correct the date. The date must be in yy/mm/dd or yy-mm-dd format.
<I>	Displays the site information.
<J>	Set detector number.
<N>	Allows the user to set the site location name
<P>	Allows new password to be set.
<R>	Resets HBD. (The same as manual reset switch on front of HBD.
<S>	Allows user to set status point information.
<T>	Allows the user to view the time and date with the option to correct the time. Time must be in hh:mm:ss. Seconds are optional format.
<V>	Displays the time of the last power-up.
<H> <M>	Turns off the HBD radio.
<H> <U>	Turns on the HBD radio.
<H> <D>	Disables the HBD.
<H> <E>	Enables the HBD.
<Y>	Selects the type of heats displayed.

Mode:

<C>	Displays the current alarm level settings as well as the minimum and maximum values that the settings may take.
<A>	Allows the user to specify the number of alarms.
<C> <A>	Sets Car Side Slope Adjustment.
<C> <L>	Sets Car Side Low Limit.
<L>	Sets Hot Bearing Low Limit.
<H>	Sets Hot Bearing High Limit.
<W>	Sets Hot Wheel Limit.

Following are examples of each listing/display offered by the DCP Alarm Mode and how to read the data.

***** <C>urrent Levels command *****

This command sends a message to the detector requesting the current alarm levels stored. The detector responds with the current levels which are displayed as follows.

```
A>C
Railroad Name          MILEPOST: 1234.5
**** HBD/HWD v3.8 DCPx v3.1
--HBD/HWD current alarm levels--Current--Minimum--Maximum--
Hot bearing low limit      9.0      5.0      12.0
Hot bearing high limit    18.0     15.0     14.0
Car side slope adjust      1.33     0.68     2.36
Car side low limit         8.0      5.0     15.0
Hot wheel limit           12.2      8.0     24.0
Maximum number of alarms      7        5        12
```

If the detector does not respond within a given period of time, a message is displayed indicating the DCP's inability to get the requested information. The most recent alarm levels are then printed as shown above.

***** Set Commands *****

The remaining commands in this mode allow the user to set parameter limits or alarm values for the HBD/HWD. Definitions and explanations for these parameters are discussed elsewhere within this document.

Each command may be entered in the standard command line entry format. This means that the desired limit or alarm value should be entered on the same line as the function command. For example, to change the parameter for the maximum number of alarms to 10, the user would enter the value as follows:

***** re-oot command *****

This command allows the user to reboot the HBD from the DCP terminal. The reboot will not retain any values stored in the HBD memory. All information stored will be cleared or reset to default settings. This is the same as if the "RESET" and "Data Advance" switches had been pressed from the HBD front panel.

***** Self-<C>heck command *****

This command initiates a self-test of the DCP verifying the firmware (program) checksums, check memory, and operation of some of the communication ports. If the HBD is busy sending train data to the DCP when this command is issued, the message "HBD BUSY - CANNOT PERFORM SELF-CHECK" will be displayed.

After completion of the self-test, one of several messages may be printed giving the results of the test. "SELF CHECK OK" indicates that the DCP has passed all tests. The other messages are as follows:

"BIOS ROM"	meaning that the BIOS firmware checksum is bad.
"PROGRAM ROM"	meaning the program checksum is bad.
"PORT n"	meaning that port number n is bad.

***** <D>ate command *****

This command allows the user to view the date as currently stored by the HBD and then be prompted to set a new date. If the date stored is correct, simply press <RETURN> and the current date will be unaffected. If the date is incorrect, enter a new date in the form of yy-mm-dd or yy/mm/dd. The new date is immediately sent to the HBD and confirmed.

***** <I>nformation command *****

This command is identical to the I command found in the Display Mode. It is included here as well to allow easier verification of site data changes available in this mode.

***** <J> command *****

This command allows the user to specify a detector number for the DCP. A unique detector number is only used at sites where two hot box detectors are installed for a double track system and the DCPs are going to share one modem. When the DCPs have been identified with unique detector numbers, the software for each DCP will not respond to a remote user until an identification string has been input by the user. The identification string consists of pressing

the <Ctrl> key and the <G> key simultaneously and then entering the detector number. The DCP with that number will then respond with the standard signon message described at the beginning of this chapter. To access the other DCP, enter an <Q> command followed by the <Ctrl> <G> sequence and the new detector number. This sequence can be performed only one time per connection.

***** <N>ame command *****

This command allows the user to enter a site name of up to 24 characters. These characters may be any printable ASCII characters. Once the site name has been accepted, the DCP will verify the change to the user by displaying the new name.

***** <P>assword command *****

This command allows the user to set or change the existing password. The user will be prompted to enter the new password TWICE to assure an accurate password setting. If both the new passwords are not the same, the new password will not be accepted and old password will still be in force.

On initial power-up of the system, the password is set to a NULL string (meaning nothing) to allow access to the Maintenance Mode where the password is set. If a password has been set no access to all other modes will be denied from the Display Mode.

DO NOT FORGET THIS PASSWORD!

The only way that a password can be cleared is by clearing all RAM. This is done by removing jumper W5 on the DCP board. Once this jumper has been removed all memory will be erased. It is important to retrieve any necessary data from memory before this jumper is removed. Once RAM has been cleared reinstall the jumper to its original position.

***** <R>eset command *****

This command is used to reset the HBD. It provides the same function as if the "RESET" switch on the front panel had been pressed manually. If the HBD is sending train data to the DCP, the command will be ignored. When a reset does occur, it will usually be a few seconds before the cursor returns ready to accept another command.

***** <S>ite Status command *****

This command allows the user to set site status information for points 1 through 8. The user will be prompted for site number, site name, an ON message, and an OFF message. If the site number is not between 1 and 8, an "INVALID SITE NUMBER" message will be printed. For more information on site status points refer to the Site Status section later in this chapter.

***** <T>ime command *****

This command allows the user to view the time as currently stored by the HBD and then be prompted to set a new time. If the time stored is correct, simply press <RETURN> and the current date will be unaffected. If the time is incorrect, enter the time in the form of hh:mm:ss or hh:mm. The new time is immediately sent to the HBD and confirmed.

***** <V> command *****

This command displays the time and date that the HBD system was last powered-up.

***** <H>BD <M>ute command *****

This command is used to turn off the HBD radio transmissions. Once the command has been entered, the user will be asked to verify the command before it is executed. If a train is passing the detector at the time this command is executed, the DCP will notify the user and ask if it is desired to continue the command. The DCP then sends a message to the HBD instructing it to not transmit all subsequent train messages.

If the radio has been muted, a message stating such is included in the report from the I command found in the Maintenance and Display Modes. If the radio was muted during a train passage, a message is included in the reports produced by the R, D, and A commands found in the Display Mode.

***** <H>BD <U>nmute command *****

This command is used to turn on the HBD radio transmissions. Once the command has been entered, the user will be asked to verify the command before it is executed. A message is then sent to the HBD telling it to transmit all subsequent train messages over the radio.

***** <H>BD <D>isable command *****

This command allows the user to disable the HBD. The DCP will function normally but the HBD will not process any trains, real or test. Some commands in the Maintenance and Display Modes will not function if the detector has been disabled. They will respond with the message stating the HBD is disabled. The HM, HU commands from the Maintenance Mode and the T command from the Display Mode respond in this manner.

***** <H>BD <E>nable command *****

This command allows the user to enable the HBD. The HBD will start processing real and test trains. If a real train is passing when this command is issued, it will be processed from the time the detector was enable and will probably fail integrity.

***** <Y> command *****

This command allows the user to select the type of heat units to be displayed. There are three available heat types: millimeters, degrees Farieheit, and degrees Celcius.

Modem Operation

To ensure proper operation of the DCP call-in feature, Harmon Electronics recommends the use of the MultiTech 224E 2400 Baud Modem. If a modem made by any other manufacturer is used, please contact Harmon Electronics, Inc. before installing the modem. Some modems are not recommended by Harmon Electronics, Inc. and may not operate correctly with the DCP and, therefore, become the sole responsibility of the user.

Two sets of DIP switches are located on the bottom of the MultiTech 224E unit, one has eight switches, the other has four. Proper setting of these switches is necessary for the modem to operate properly. Figure X.3 shows the required settings. Note the orientation of the individual switches with respect to the modem. A closed setting is indicated by the switch be placed in a position pointing down into the modem while an open setting is indicated with the switch pointing up out of the modem.

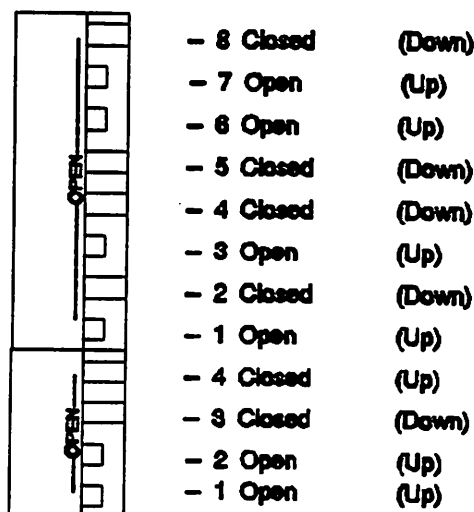


Figure X.16

When the DCP software is initialized, the modem is also initialized with a command string. Whenever the modem's Ring Indicate line goes active, the DCP will detect the incoming call and cause the modem to answer. As soon as the call is completed, the DCP re-initializes the modem and gets ready to receive another call.

Site Status

The DCP has the capability of reading eight external TTL level inputs. By connecting a dry contact closure to the external terminals, the DCP can at any time read the state of the closure. These inputs could be used for a variety of applications including a open door indicator or battery power sensor relay.

For the DCP III, the terminal connection strip is located on the back of the HBD/HWD cabinet; on the DCP II series, the terminals are on the back of the DCP II rack. NOTE: DO NOT connect any live power to the terminal strips unless approve by Harmon Electronics, Inc. engineering or technical personnel.

Using the S Command from the Display Mode, the user can find out the current status of any of the established points. The display will either show ON or OFF depending on the status of the contact closure. In the Maintenance Mode, the S Command allows the user to specify a sixteen character name for each status point. This allows for easier identification of the individual sites.

HBD Interface

A communications pathway does not inherently exist between the HBD/HWD and the DCP; the DCP III does not accept signals from the backplane and the DCP II is physically isolated in another rack. Therefore, a communications pathway must be created to allow information to transfer back and forth from the DCP. This is accomplished via a male DB-25 terminated cable attached to the Time and Date Board of the HBD/HWD. A data transfer protocol has been implemented to minimize the possibility of data corruption.

DCP-II Physical Parameters

The DCP-II consists of a twelve slot Standard (STD) Bus chassis with four STD cards (six for the DCP-II+). Harmon Electronics manufactures the Accessory Board for the DCP-II and the circuit description for this board is discussed in the Hardware Reference portion of this document. Part of the function of the Accessory Board is the configuration of the serial communication ports which is described below.

<u>Designation</u>	<u>Name</u>	<u>Use</u>
J1	LOCAL	Connect to local terminal or printer
J2	HBD	Connect to HBD time/date board
J3	REMOTE	Connect to MultiTech 224E modem
J4	AUX	Same as Local port

	<u>Local</u>	<u>HBD</u>	<u>Remote</u>	<u>Aux</u>
Type	DCE*	DCE*	DTE*	DTE*
Buad Rate	**	9600	1200	***
Word Length	**	8	8	***
Parity	**	None	None	***
# Stop Bits	**	1	1	***
Handshake	XON/XOFF	CTS	XON/XOFF	XON/XOFF

* Jumpers JD2 and JD3 on the Accessory Board are used to determine the communications parameters of the LOCAL port as given as follows:

Jumper position	<u>JD2</u>	<u>JD3</u>	
	OFF	OFF	300 baud, 7 bit, odd parity
	ON	OFF	300 baud, 7 bit, even parity
	OFF	ON	1200 baud, 8 bit, no parity
	ON	ON	9600 baud, 8 bit, no parity

** Jumpers JD5 and JD6 of the Accessory Board are used to determine the communications parameters of the AUX port as given as follows:

Jumper position	<u>JD5</u>	<u>JD6</u>	
	OFF	OFF	300 baud, 7 bit, odd parity
	ON	OFF	300 baud, 7 bit, even parity
	OFF	ON	1200 baud, 8 bit, no parity
	ON	ON	9600 baud, 8 bit, no parity

An ON condition indicates the jumper has been placed across pins 1 and 2. Jumpers JD4 and JD7 are not used.

One additional item to note about the memory configuration for the DCP-II+. Two additional memory cards are added to the STD bus chasis to provide the 768k RAM. In order for the CPU to address this memory, the memory cards must have different addresses which are set via Jumper Block J11. One card must have a single jumper across pins 1 and 2, another must have have a single jumper across pins 3 and 4, and the third must have a jumper across pins 5 and 6.

DCP-3 Physical Parameters

The DCP III is a single board addon to the HBD/HWD backplane bus system. A description of the component circuits on the board has been delt with in another section of this document. However, it is important to highlight some of the more important features of the DCP III board.

There are four serial ports on the board providing a communications link between the HBD/HWD and the outside world. The location and function of these serial ports is defined in the following table:

<u>Designation</u>	<u>Name</u>	<u>Use</u>
J1	LOCAL	Connect to local terminal or printer
J2	HBD	Connect to HBD time/date board
J3	REMOTE	Connect to MultiTech 224E modem
J4	AUX	Connect to radio modem

As serial ports may be created in a variety of configurations it is helpful to define each of the DCP ports in terms of equipment type, baud rate, word length, parity, stop bits, and handshaking protocol. The following table shows how each port is configured:

	<u>Local</u>	<u>HBD</u>	<u>Remote</u>	<u>Aux</u>
Type	DCE	DCE	DTE	DTE
Baud Rate	*	9600	1200	**
Word Length	*	8	8	**
Parity	*	None	None	**
# Stop Bits	*	1	1	**
Handshake	XON/XOFF	CTS	XON/XOFF	XON/XOFF

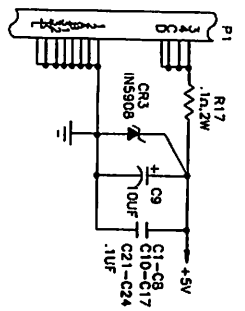
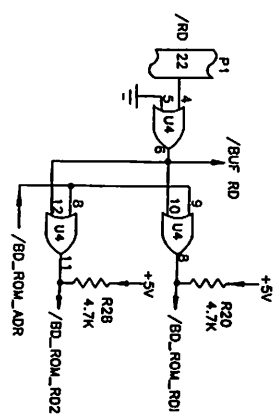
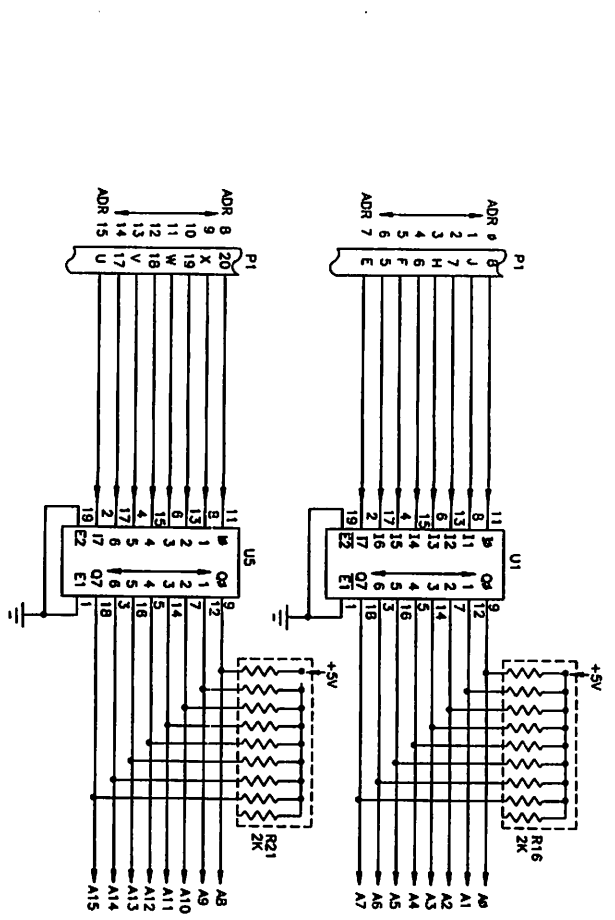
As can be seen from the table, one or more items on each port may be independently configured. All four ports may be as either DCE or DTE. The method for setting this factor is found in the Hardware Physical Description for Jumpers W1 through W4. The equipment types given in the table are the defaults.

Configurable items for the LOCAL port are marked with an astrisk ("*"). These items are configured via DIP switches one and two on the DCP III board as shown below.

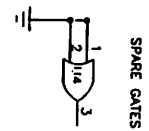
Switch	1	2	
Positions	OFF	OFF	300 Baud, 7 Bits, Odd parity
	ON	OFF	300 Baud, 7 Bits, Even parity
	OFF	ON	1200 Baud, 8 Bits, No parity
	ON	ON	9600 Baud, 8 Bits, No parity

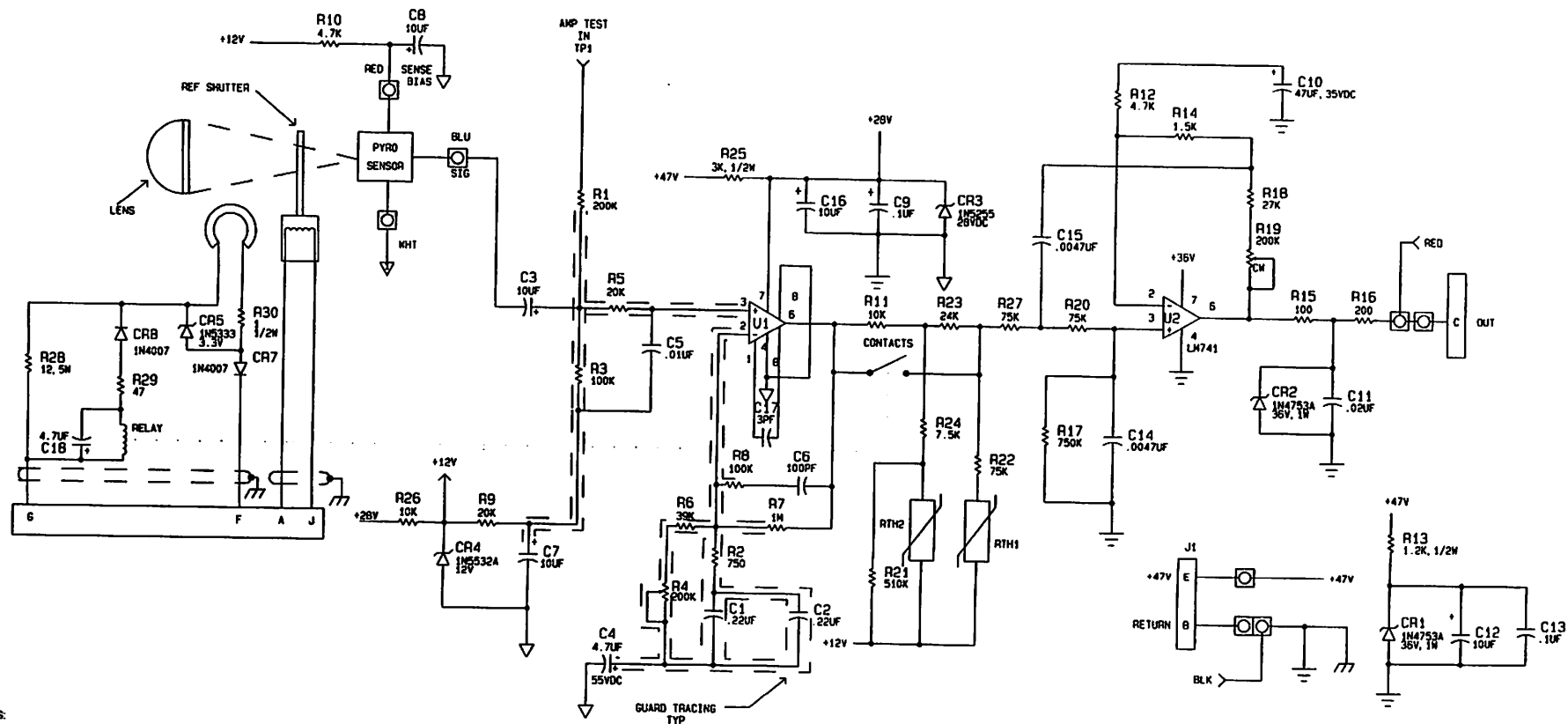
Similarly, the Aux port is configured using the DIP switches 3 and 4. These items are marked with "***" in the above table; the results are shown below:

Switch	3	4	
Positions	OFF	OFF	300 Baud, 7 Bits, Odd parity
	ON	OFF	300 Baud, 7 Bits, Even parity
	OFF	ON	1200 Baud, 8 Bits, No parity
	ON	ON	9600 Baud, 8 Bits, No parity



REF	DES	TYPE	GND	+5V
U1	LS224	10	20	
U2	LS224	10	20	
U3	LS138	8	16	
U4	LS32	7	14	
U5	LS224	10	20	
U6	LS138	8	16	
U9	LS224	10	20	

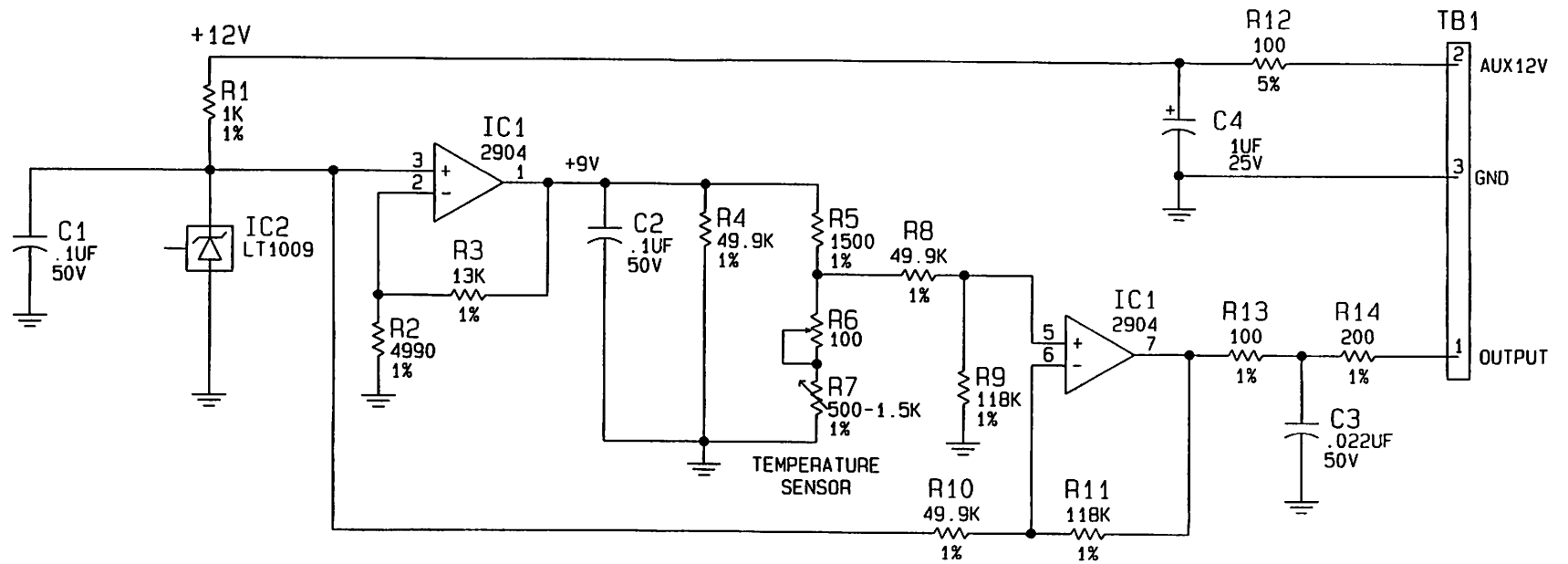




NOTES:

1. ALL RESISTORS VALUES ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS VALUES ARE IN MICROFARADS.
3. FACTORY CALIBRATED FOR 10VP OUTPUT @ 70 C DELTA.

8	ARTWORK NO.	HARMON ELECTRONICS, INC.
12	ASSEMBLY NO.	GRAIN VALLEY, MO U.S.A. 64029
16	225888-000	
18	APPROV. DATE	TITLE
20	DRAWN BY	HBD PRE-AMP
22	DRAFTING	SCHEMATIC
24	DATE	ENGINEER
26	7-26-83	C WILLE
28		DRAWING NO. 35732-000
30		SHEET 1 OF 1



ARTWORK NO. 061693-000	HARMON ELECTRONICS, INC.		
ASSEMBLY NO. 226315-000	GRAIN VALLEY, MD. U.S.A. 64029		
APPRVD. DATE	TITLE		
DRAWN BY OFR	AMBIENT_TEMP_SENSOR		
DATE 10-24-88	SCHEMATIC		
ENGINEER J. J. HOFFERBACK	DRAWING NO. 125117-000	DATE 10-24-88	BY J. J. HOFFERBACK

P1 > 14

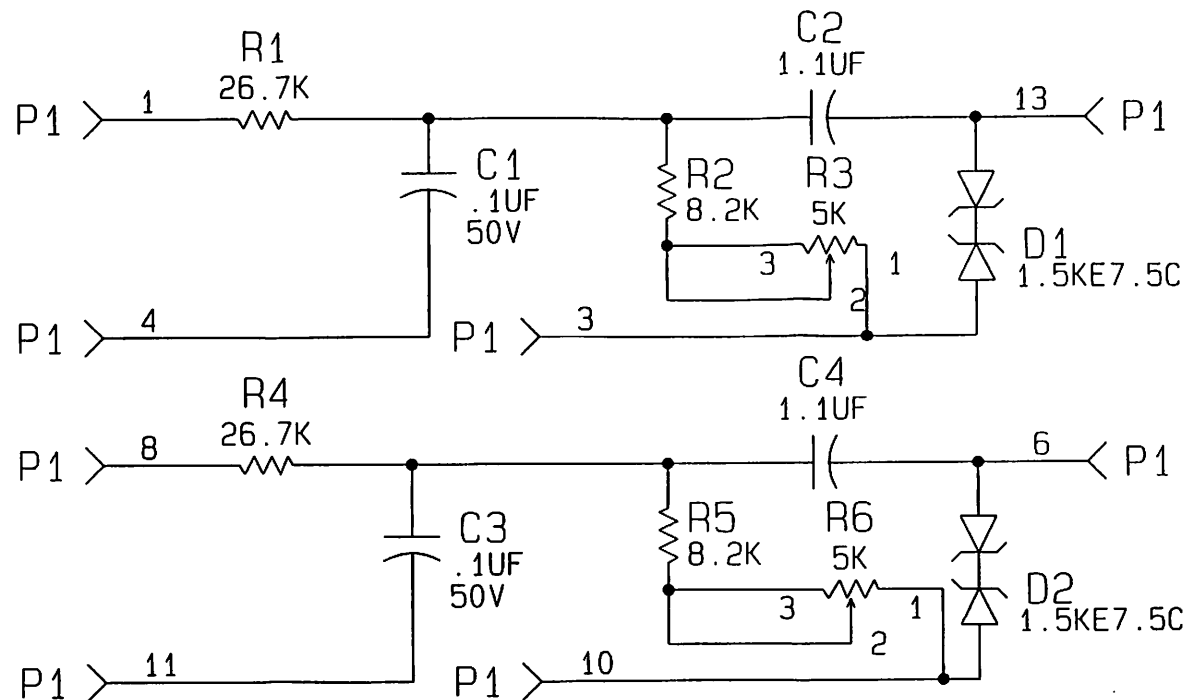
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P1 > 5

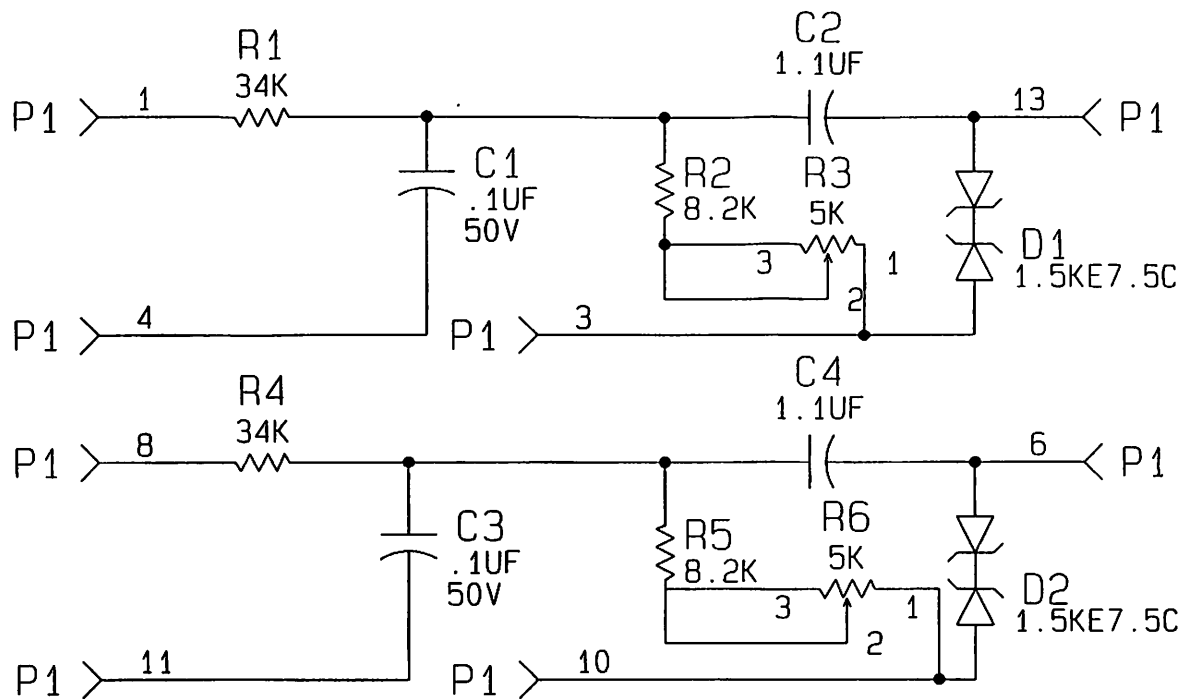
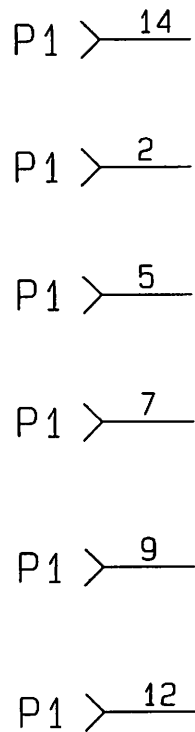
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P1 > 9

P1 > 12



		CHKD	ARTWORK NO. 61636-000		HARMON ELECTRONICS, INC. GRAIN VALLEY, MO. U.S.A. 64029			
DFR		BY	ASSEMBLY NO. 226579-000					
		DATE	APPRVD.	DATE	TITLE HBD/HWD ADJUSTABLE INPUT NETWORK SCHEMATIC			
173-2045		ECRN	DRAWN BY D.RECTOR					
			DATE					
			ENGINEER		DRAWING NO.		SHEET	



		CHKD	ARTWORK NO. 61636-000		HARMON ELECTRONICS, INC. GRAIN VALLEY, MO. U.S.A. 64029					
DFR		BY	ASSEMBLY NO. 226579-002							
		DATE	APPRVD.	DATE	TITLE GE PA100/150 ADJ. INPUT SCHEMATIC					
173-2045		ECRN	DRAWN BY D.RECTOR							
		DATE	DATE		ENGINEER		DRAWING NO.		SHEET	

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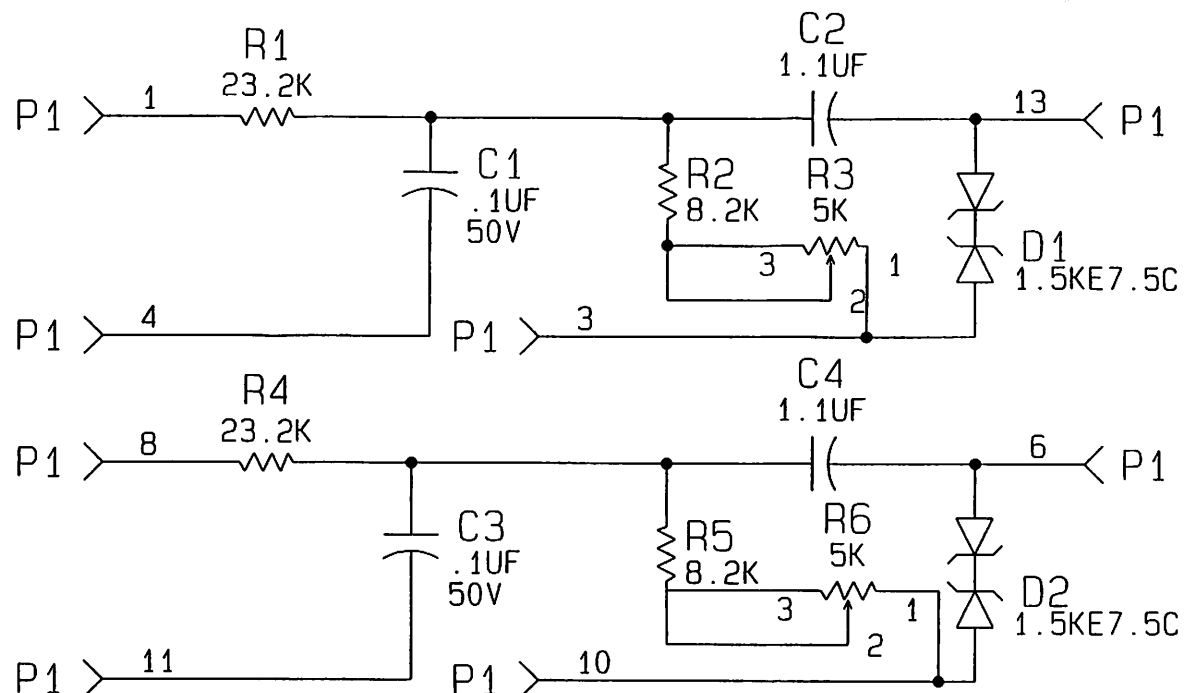
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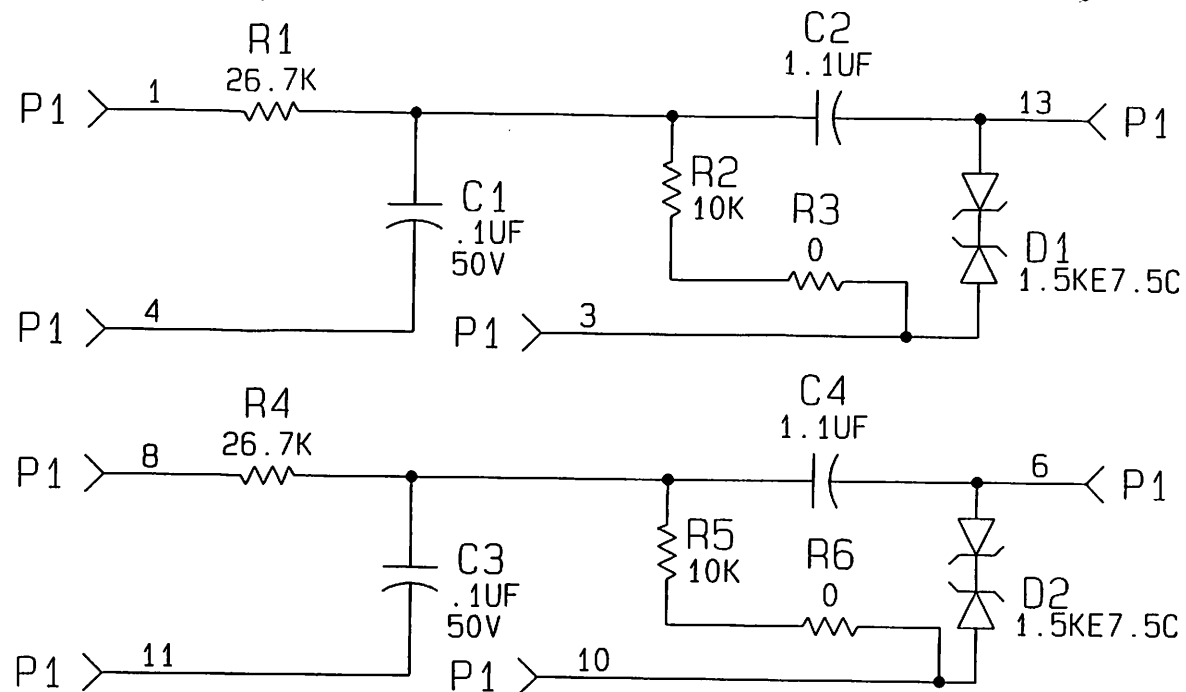
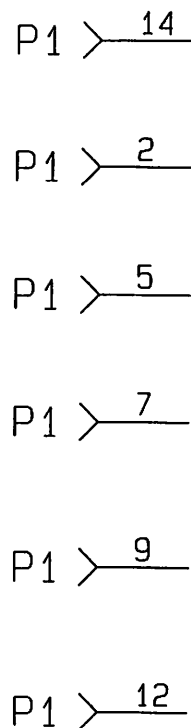
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P1 > 9

P1 > 12



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		CHKD	ARTWORK NO. 61636-000		HARMON ELECTRONICS, INC. GRAIN VALLEY, MO. U.S.A. 64029		
DFR		BY	ASSEMBLY NO. 226580-000				
		DATE	APPRVD.	DATE	TITLE HBD/HWD INPUT NETWORK SCHEMATIC		
A 173-2045		ECRN	DRAWN BY D.RECTOR				
REV		DATE	4-88		ENGINEER M. BARTONEK	DRAWING NO. 135090-000	SHEET 01 OF 1

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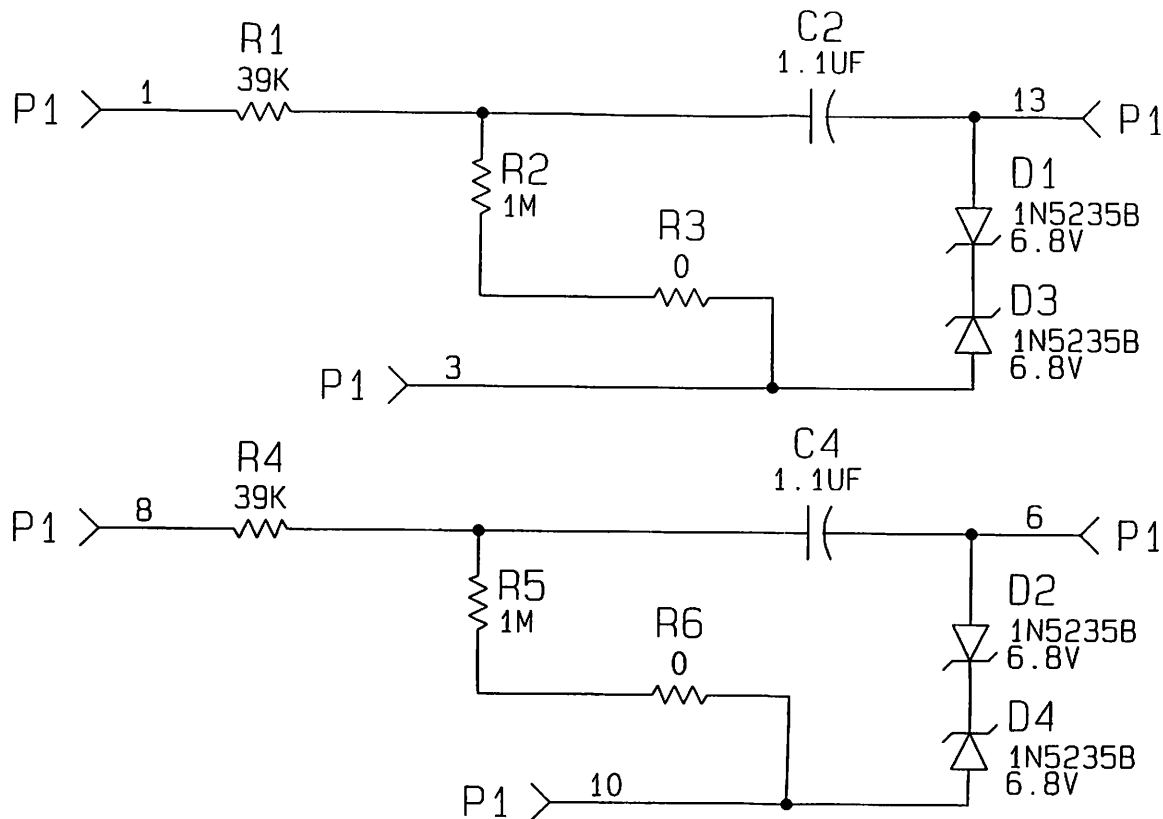
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P1 > 7

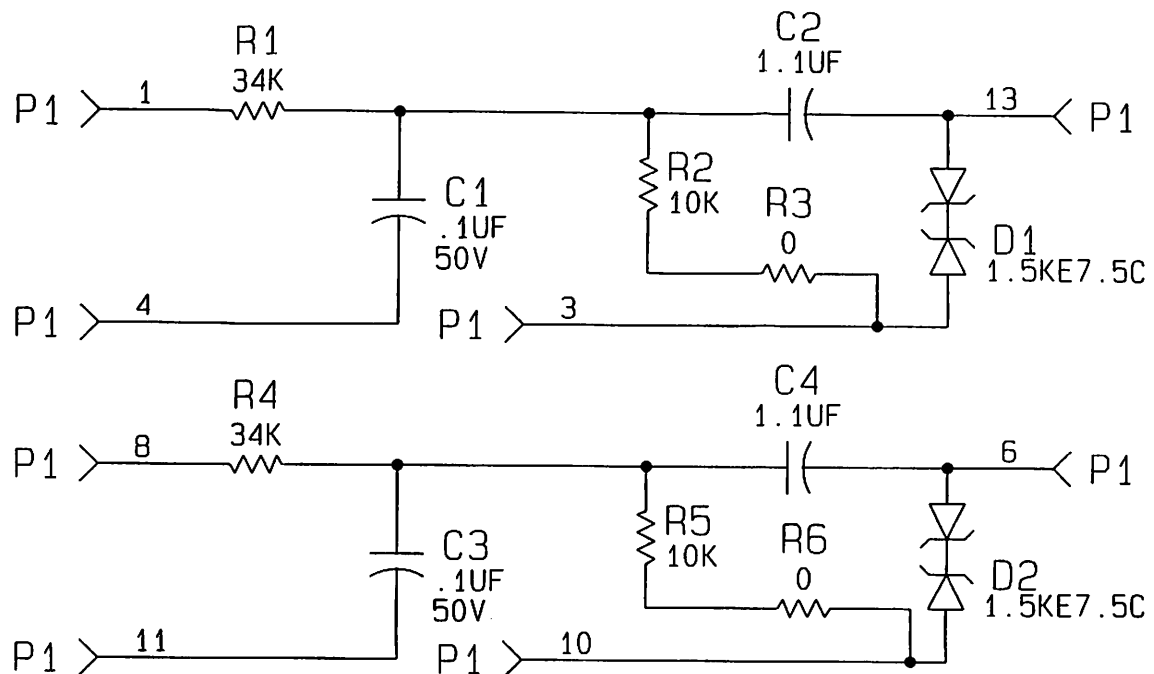
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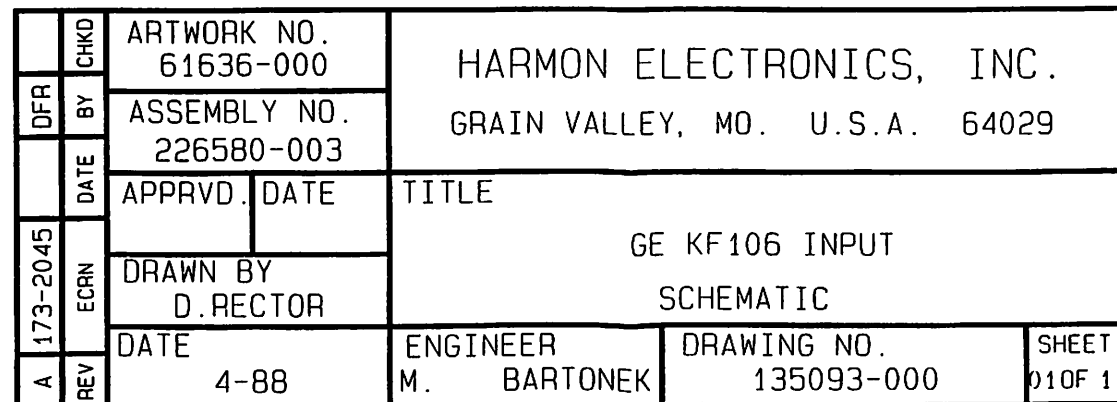


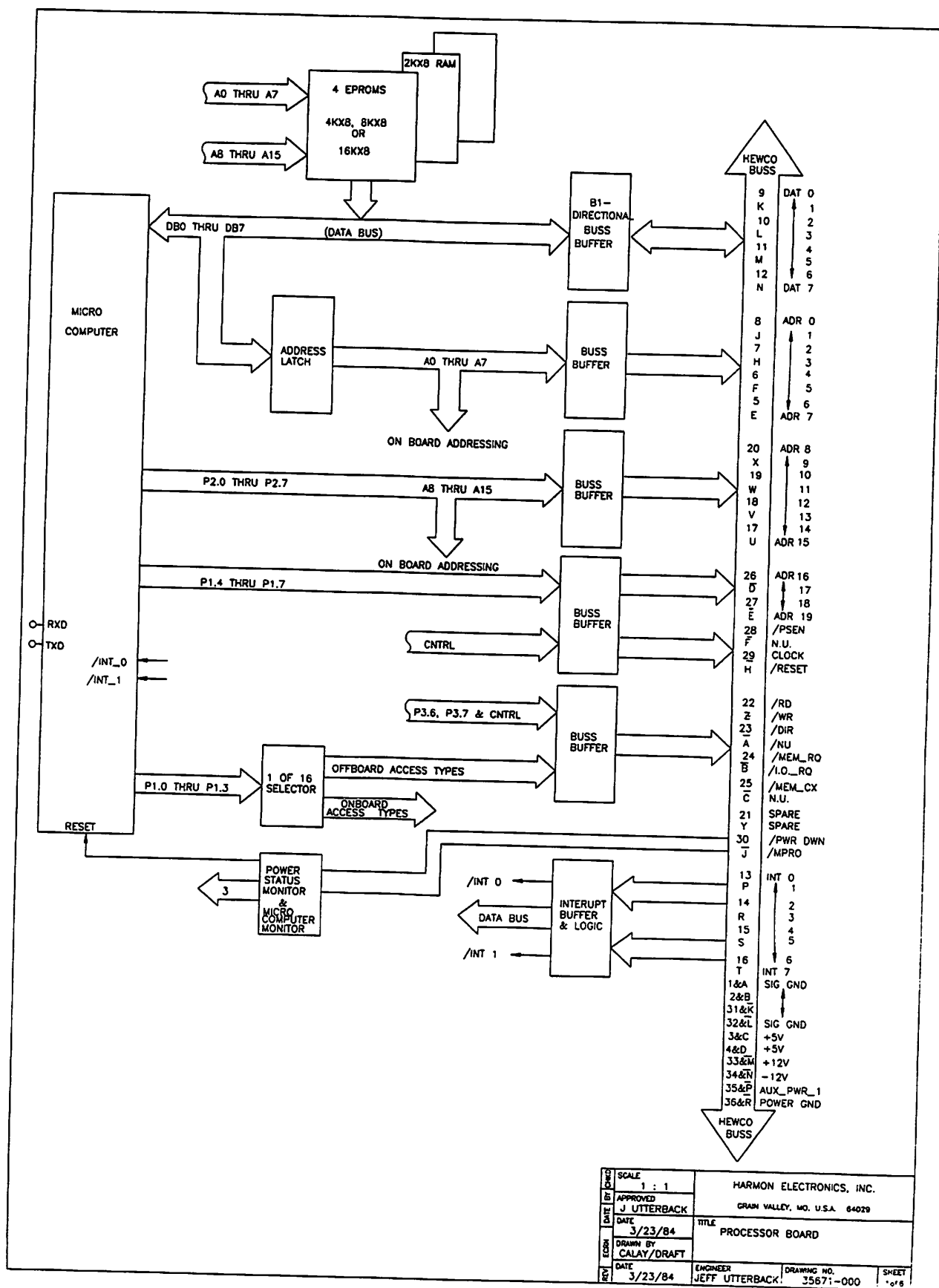
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VMD	DFR	BY	ASSEMBLY NO. 226580-001				
6/90		DATE	APPRVD.	DATE	TITLE SERVO INPUT SCHEMATIC		
164-5672	173-2045	ECRN	DRAWN BY D. RECTOR				
B	A	REV	DATE 4-88		ENGINEER M. BARTONEK	DRAWING NO. 135091-000	SHEET 01 OF 1

P1 14
P1 2
P1 5
P1 7
P1 9
P1 12

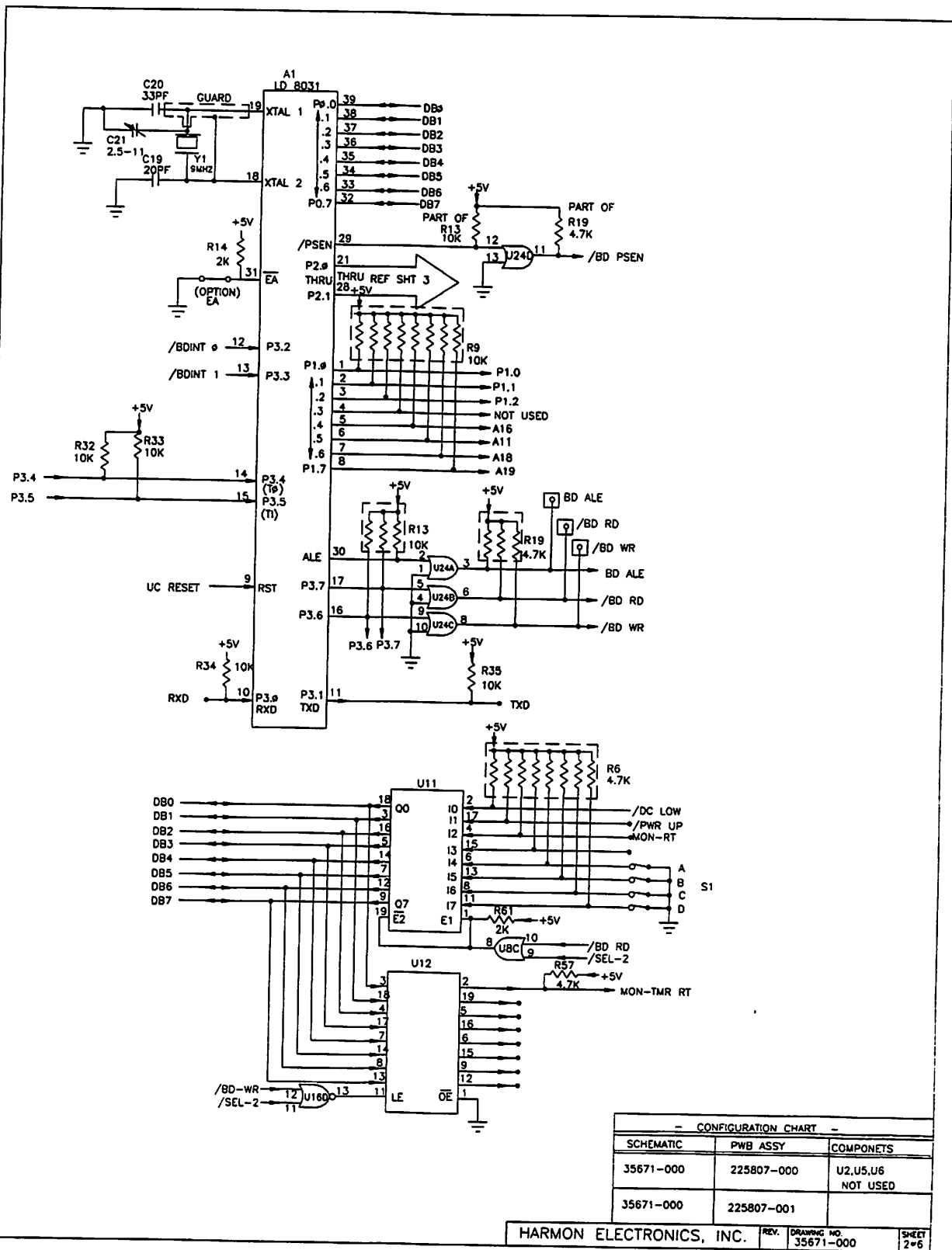


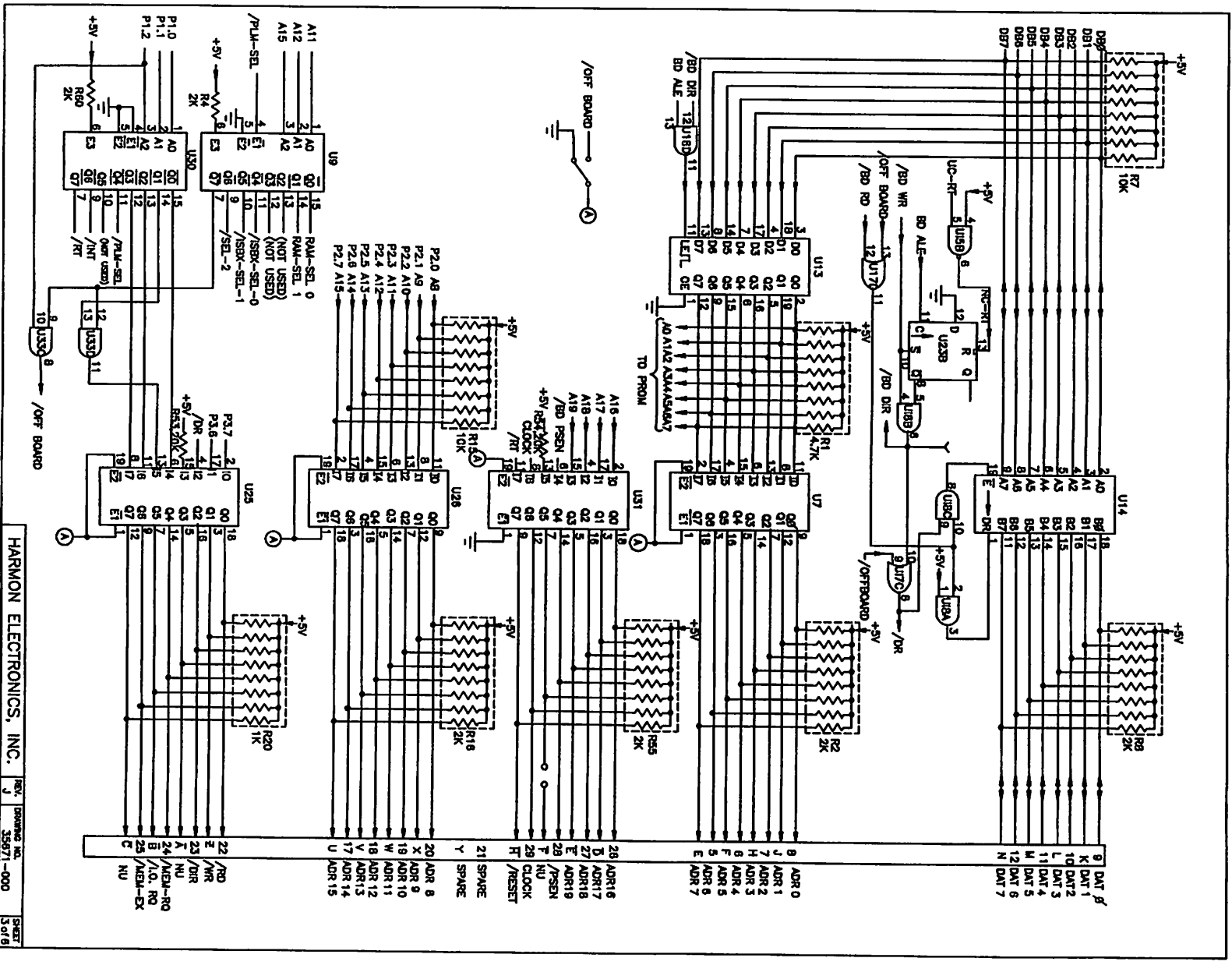
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DFR		BY	ASSEMBLY NO. 226580-002				
		DATE	APPRVD.	DATE	TITLE GEPA100/150 INPUT SCHEMATIC		
		ECRN	DRAWN BY D. RECTOR				
A 173-2045							
REV			DATE 4-88		ENGINEER M. BARTONEK	DRAWING NO. 135092-000	SHEET 01 OF 1

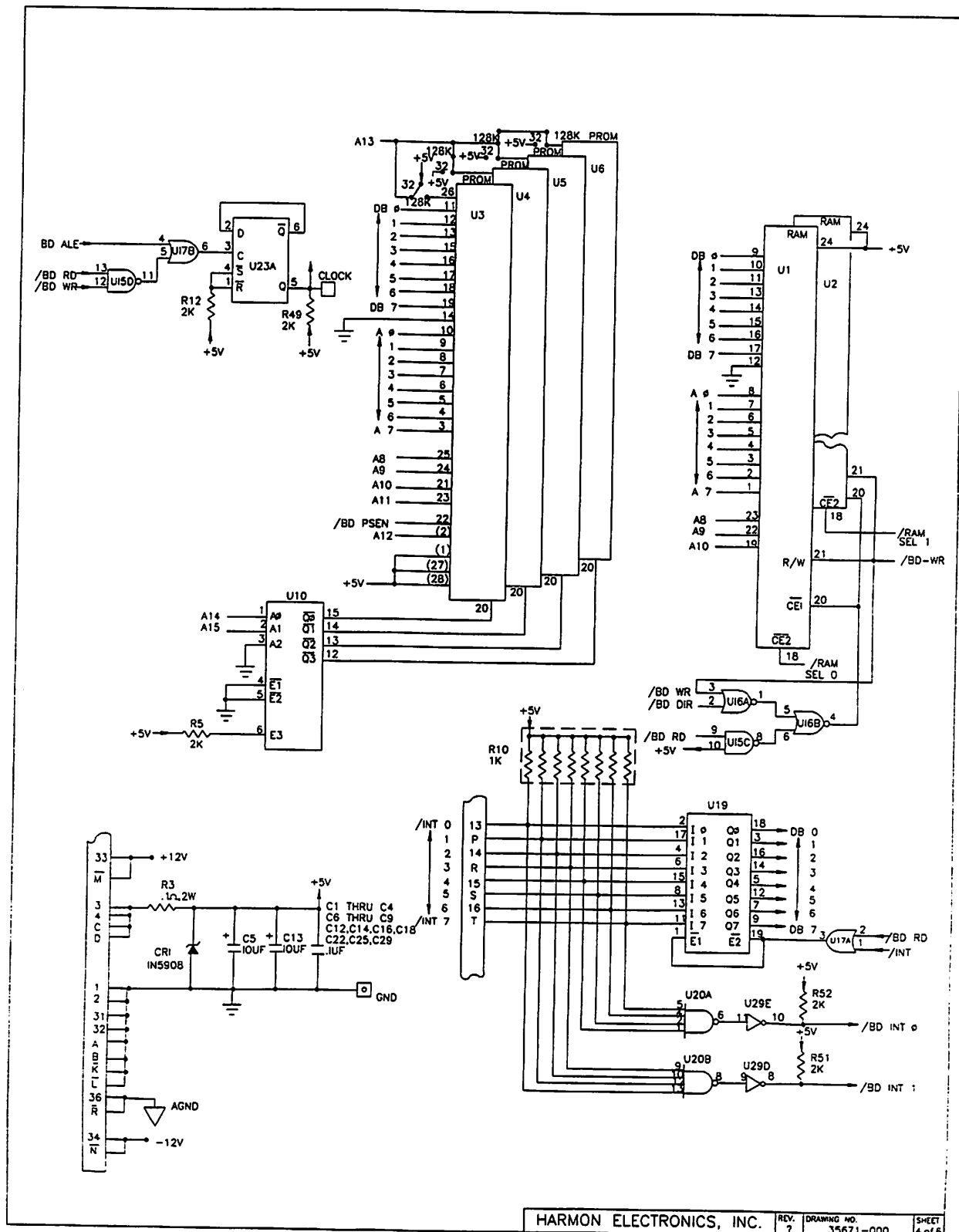


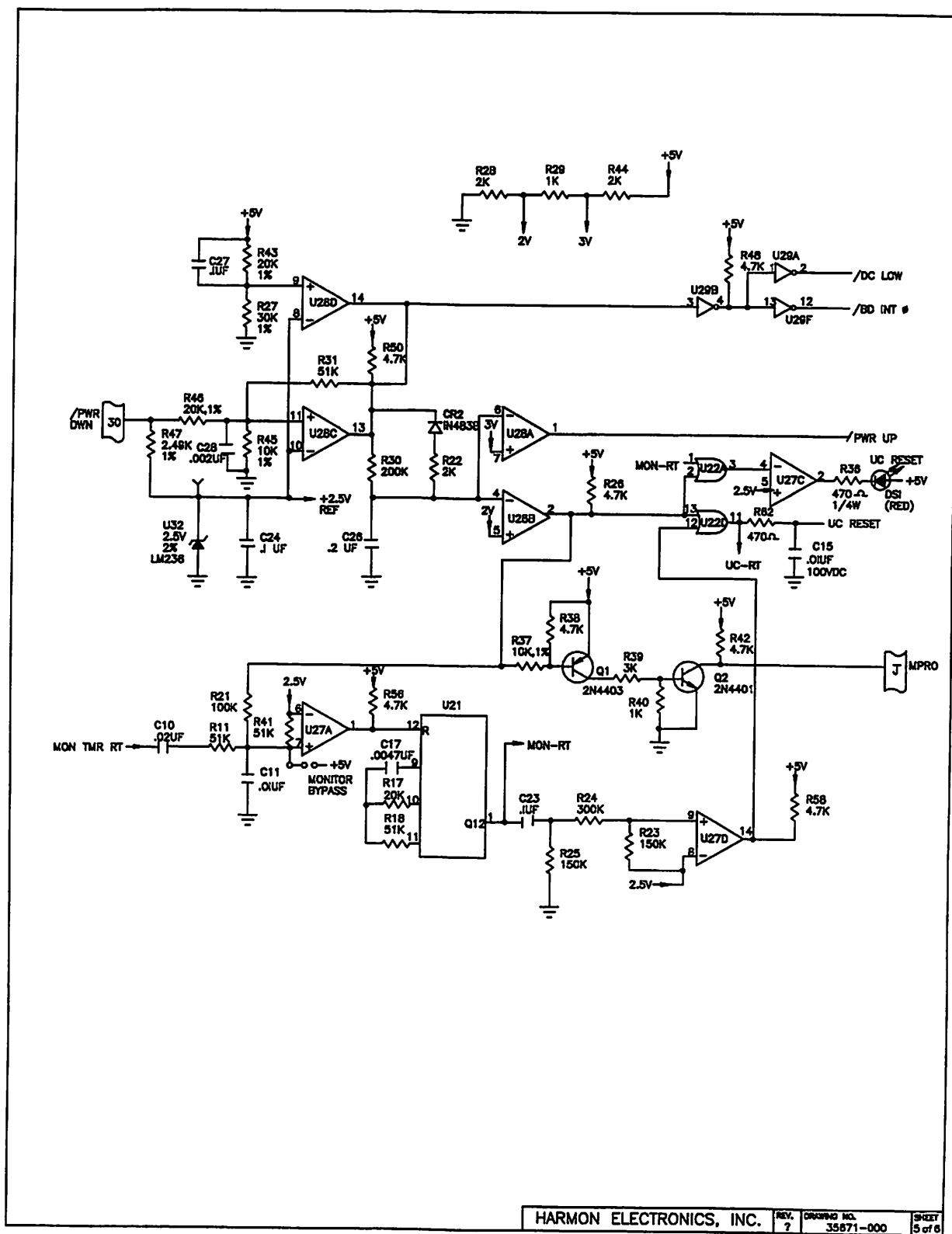


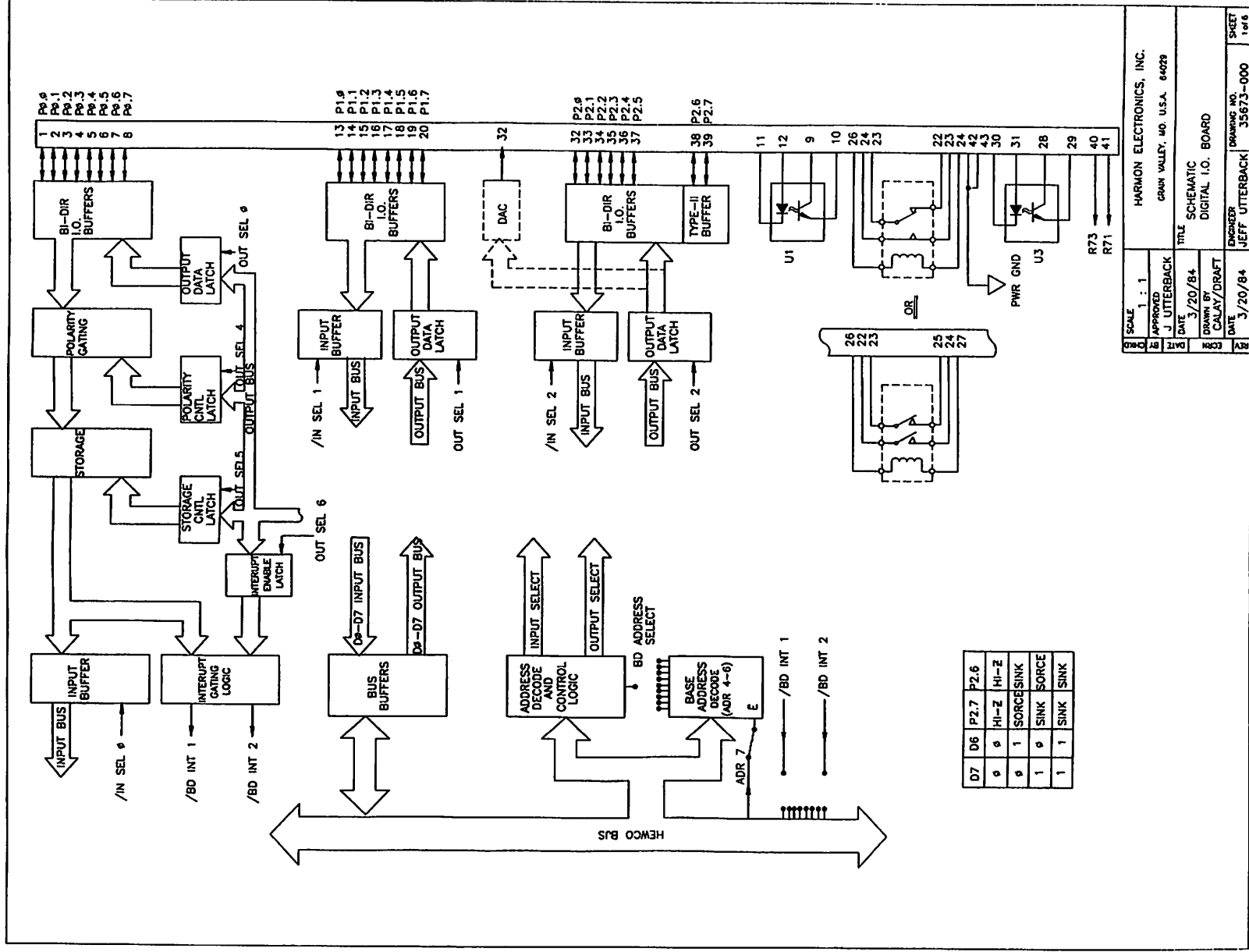
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APPROVED	J. UTTERBACK	GRAN VALLEY, MO. U.S.A. 64029	
DATE	3/23/84	TITLE	
DRAWN BY	CALAY/DRAFT	PROCESSOR BOARD	
DATE	3/23/84	ENGINEER	DRAWING NO.
		JEFF UTTERBACK	35671-000
			SHEET
			1 of 6

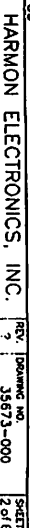


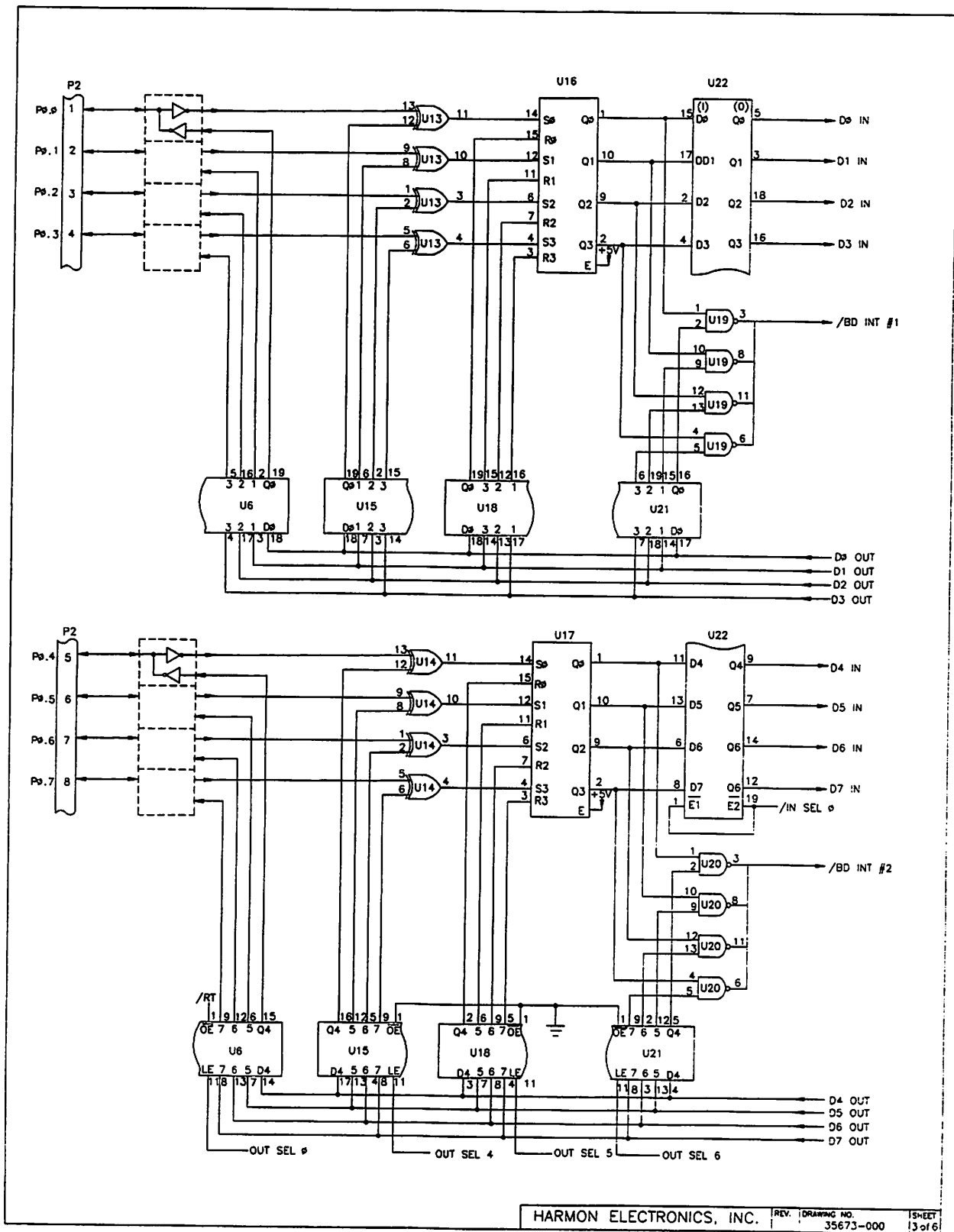




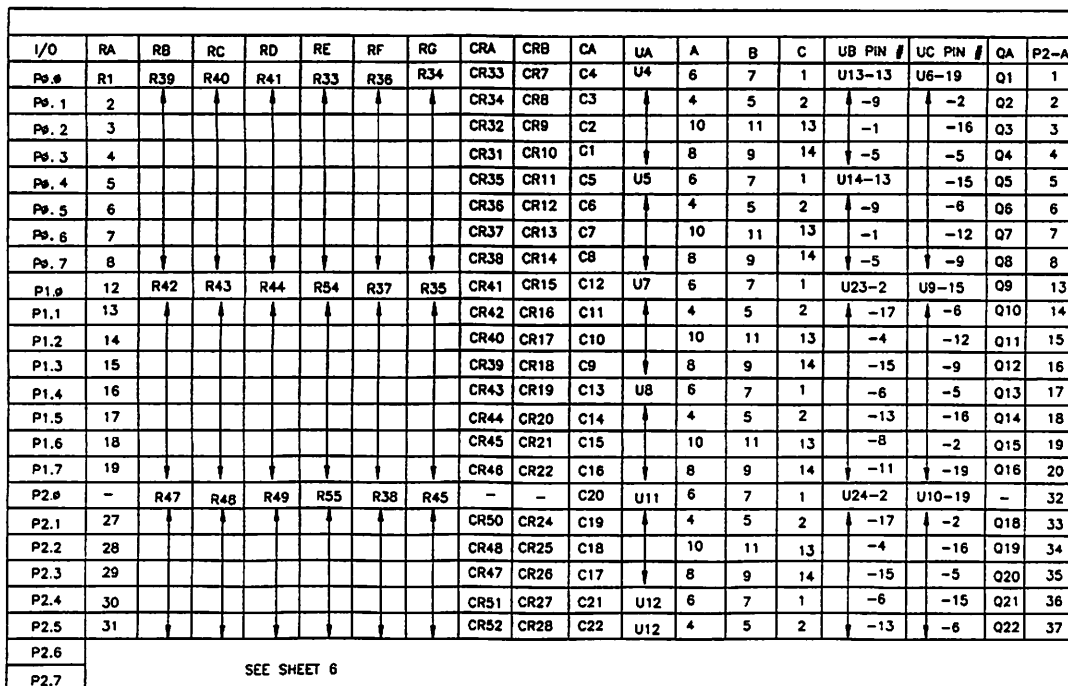
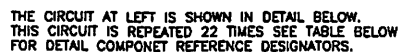


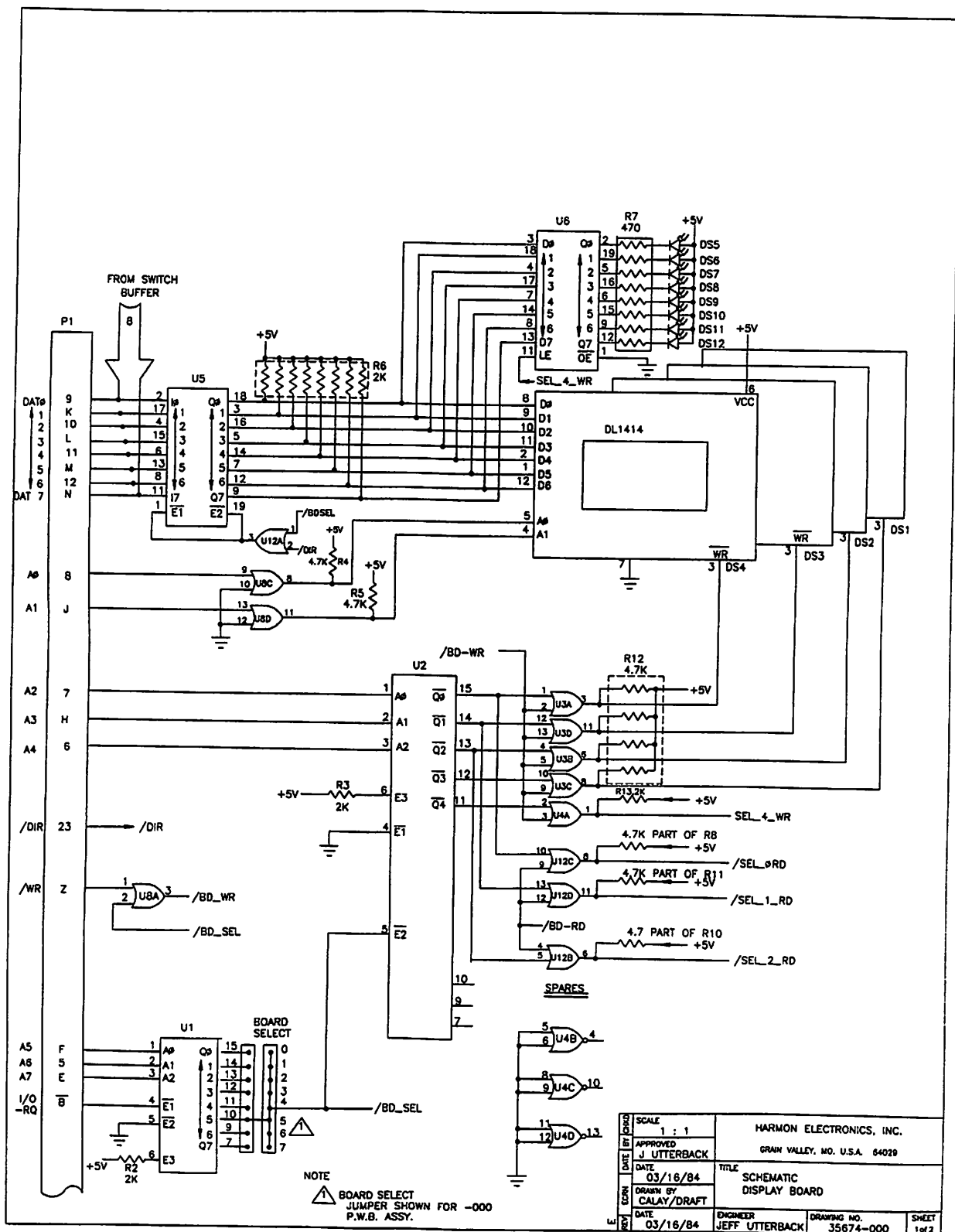




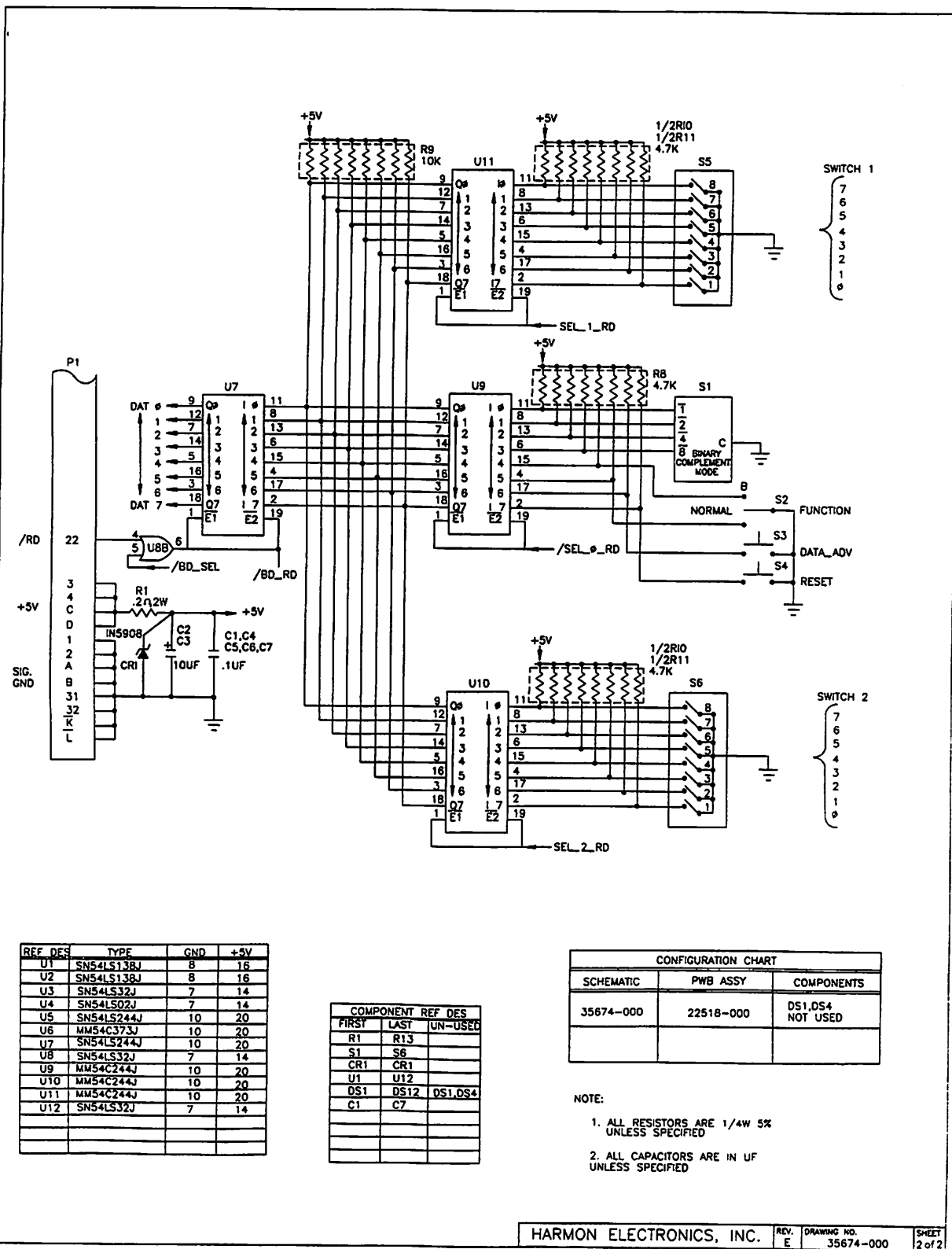


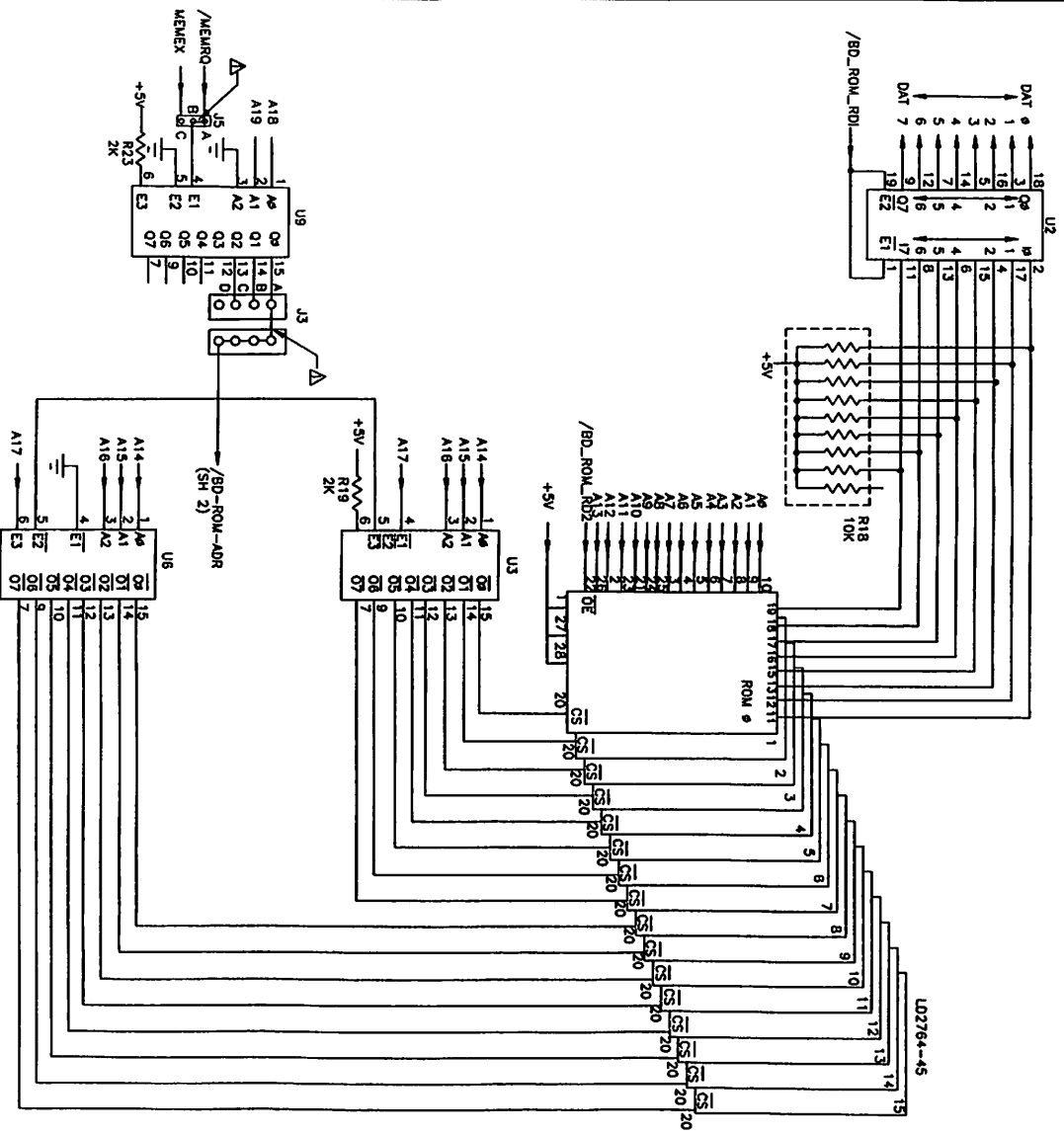




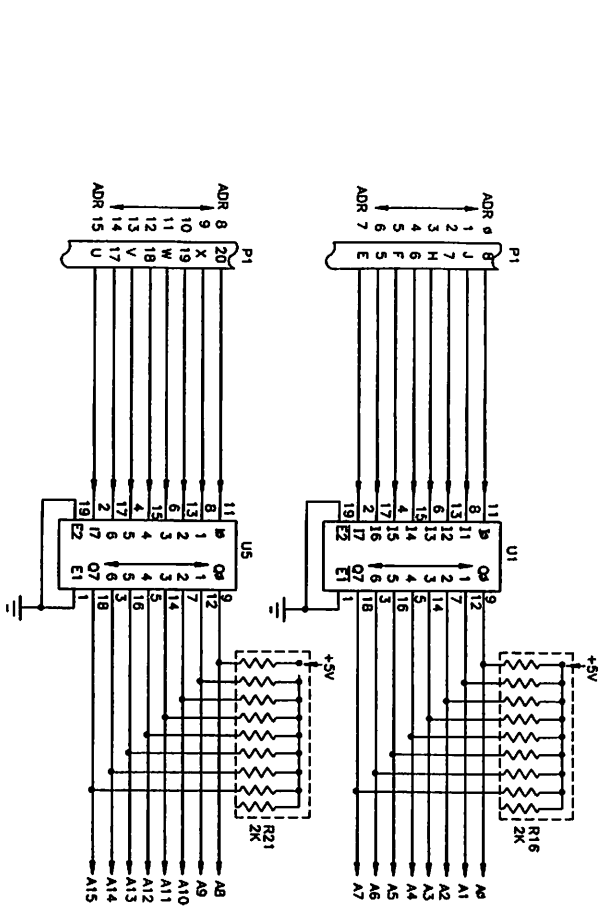


SCALE	1 : 1	HARMON ELECTRONICS, INC.	
APPROVED	J. UTTERBACK	GRAN VALLEY, MO. U.S.A. 64029	
DATE	03/16/84	TITLE	
DRAWN BY	CALAY/DRAFT	SCHEMATIC DISPLAY BOARD	
DATE	03/16/84	ENGINEER	JEFF UTTERBACK
DRAWING NO.	35674-000	SHEET	1 of 2

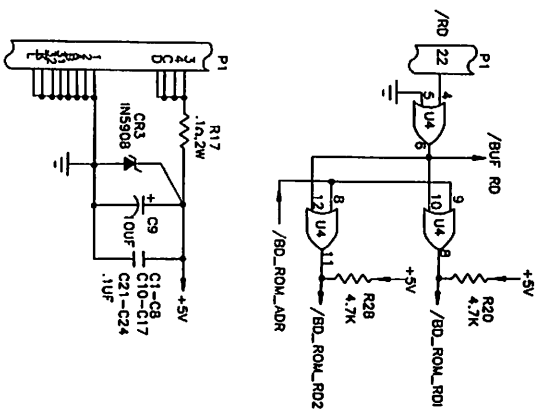
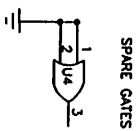


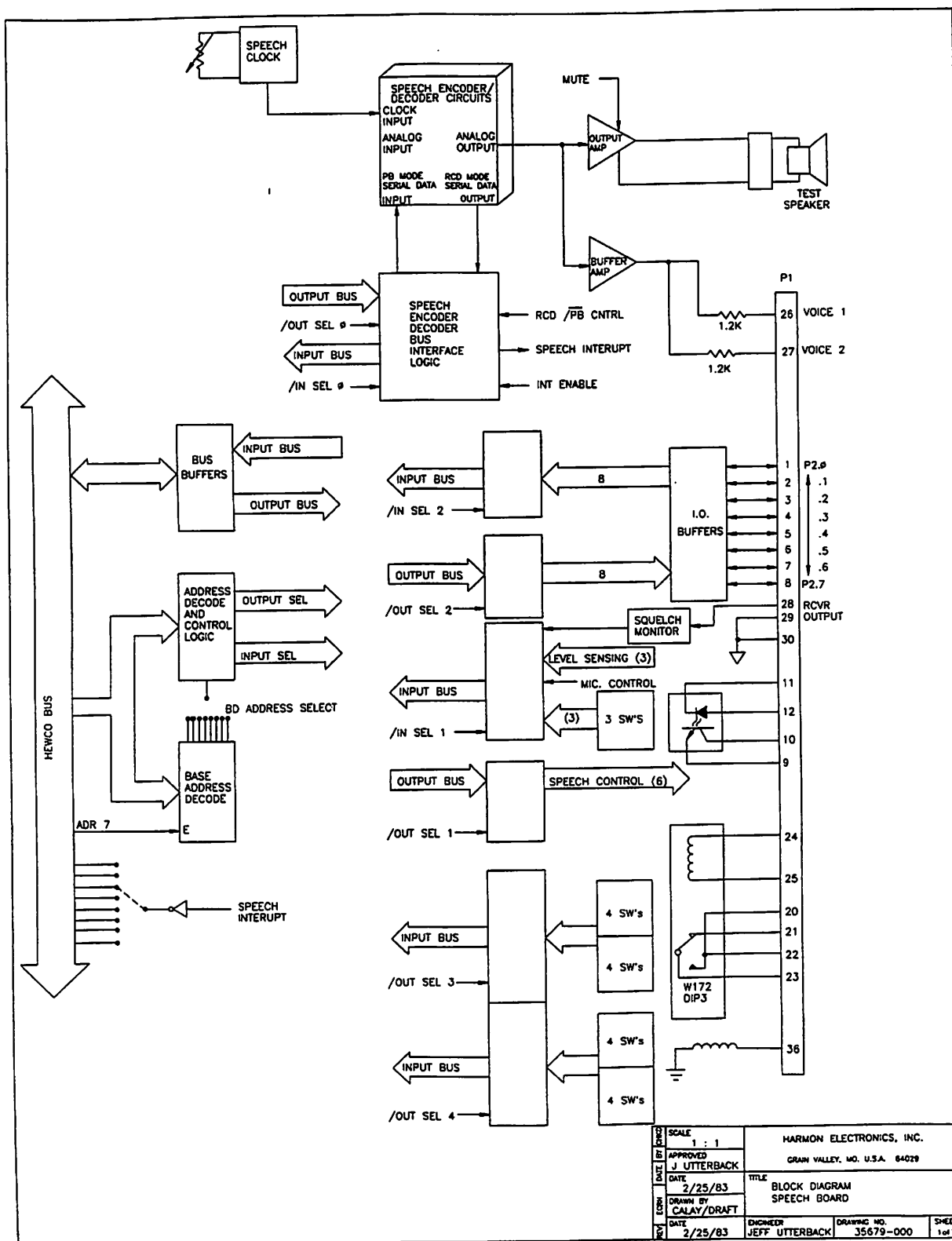


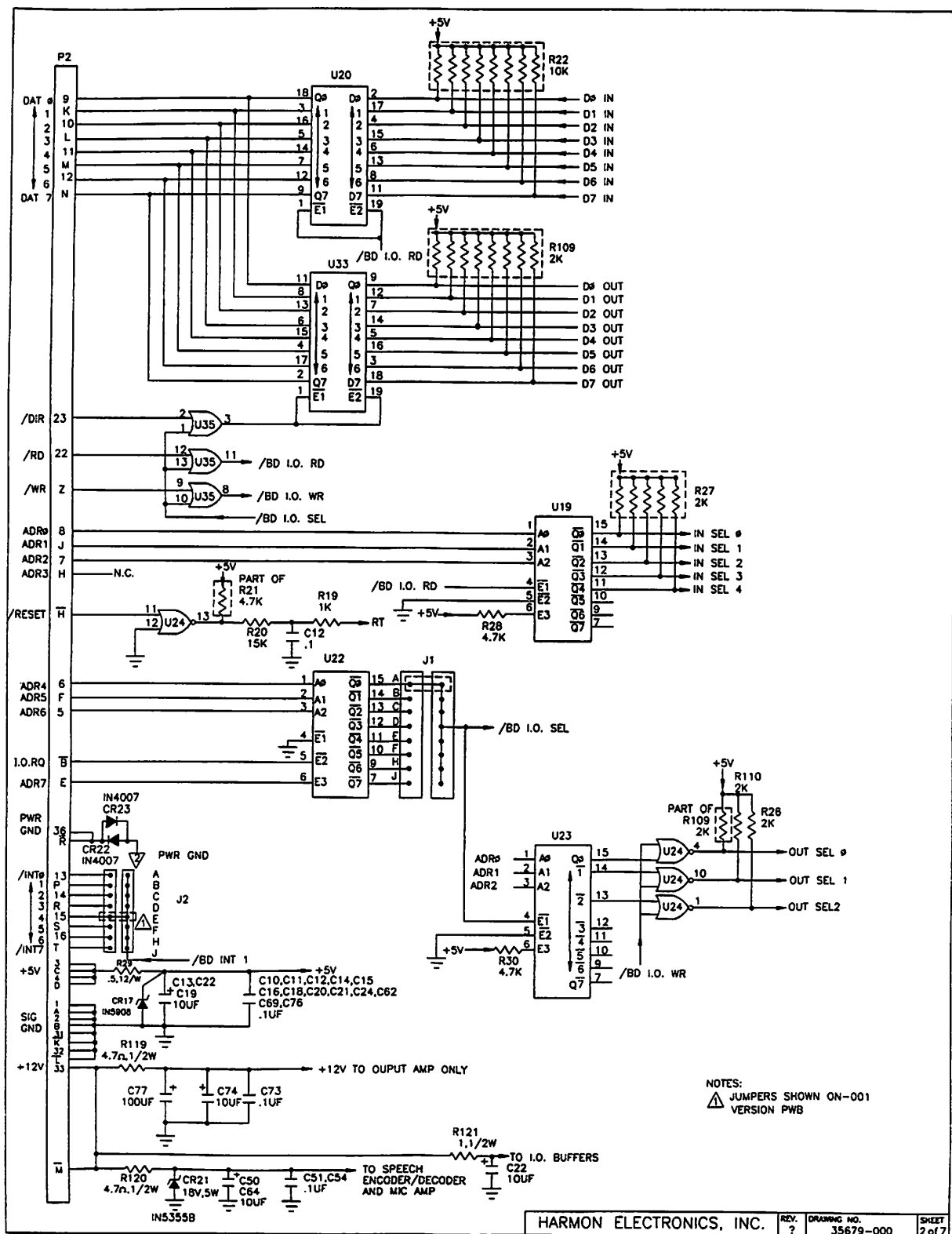
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 ▲ BOARD SELECT JUMPER
 SHOW FOR -000 PWB ASSY

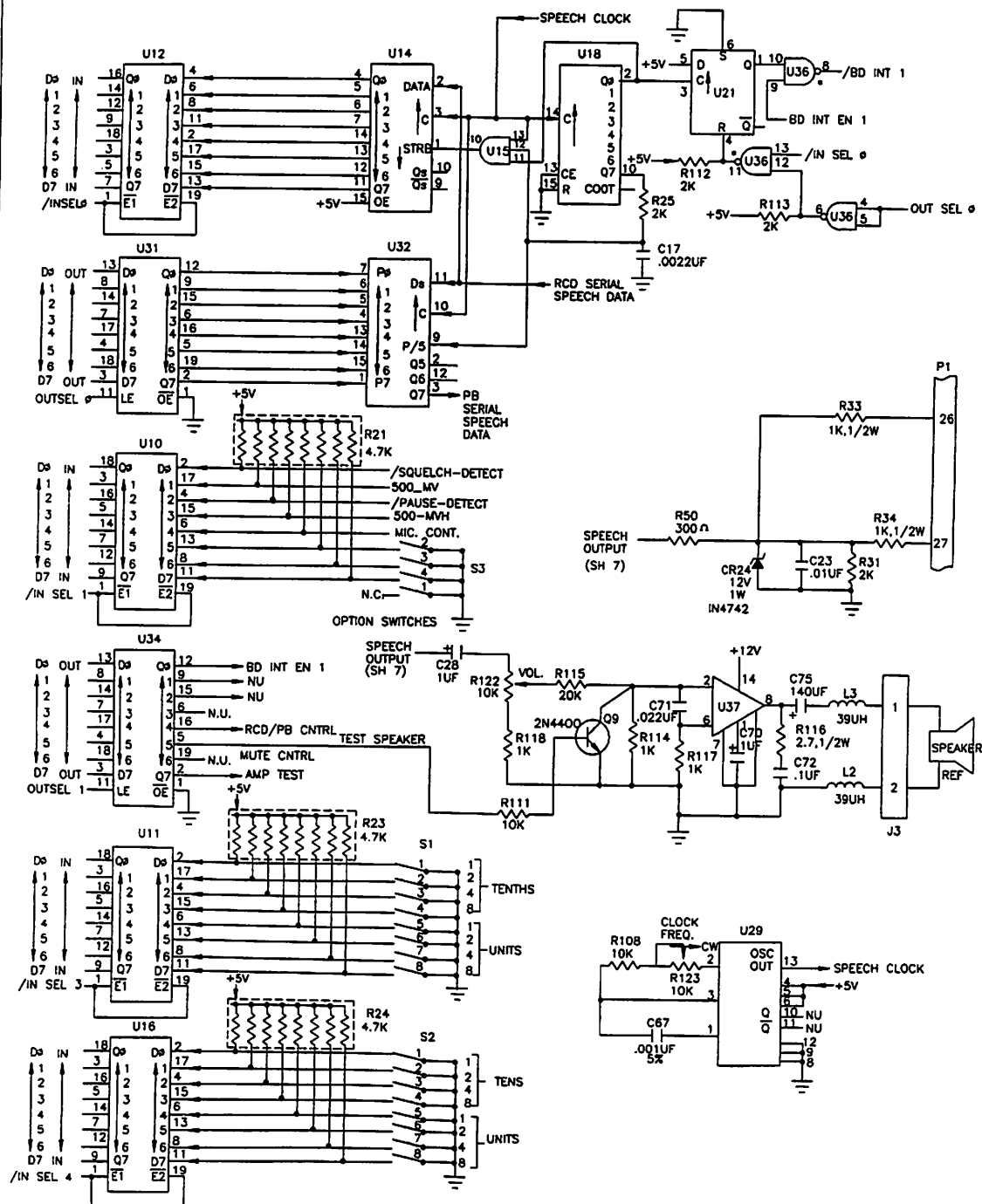


REF DES	TYPE	GND	+5V
U1	LS224	10	20
U2	LS224	10	20
U3	LS138	8	16
U4	LS32	7	14
U5	LS224	10	20
U6	LS138	8	16
U8	LS224	10	20

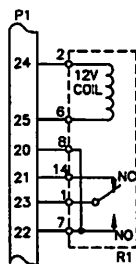
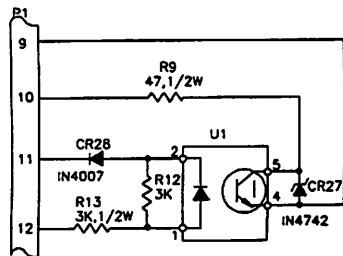








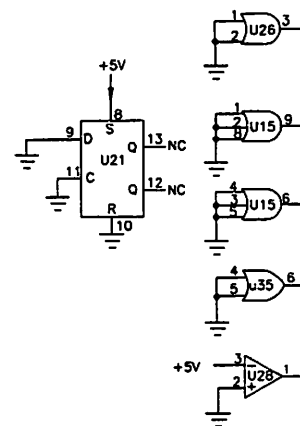




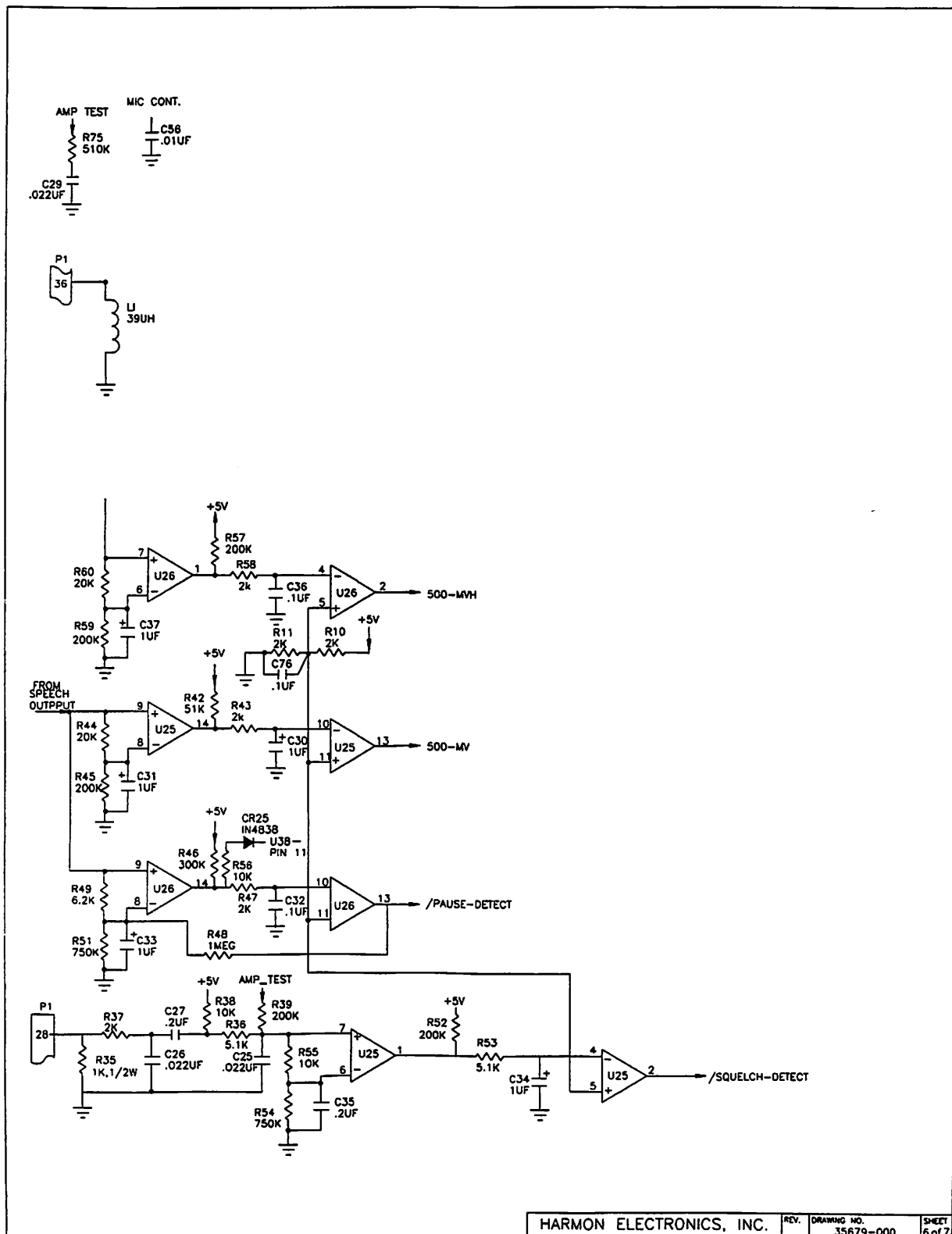
W172 DIP-3

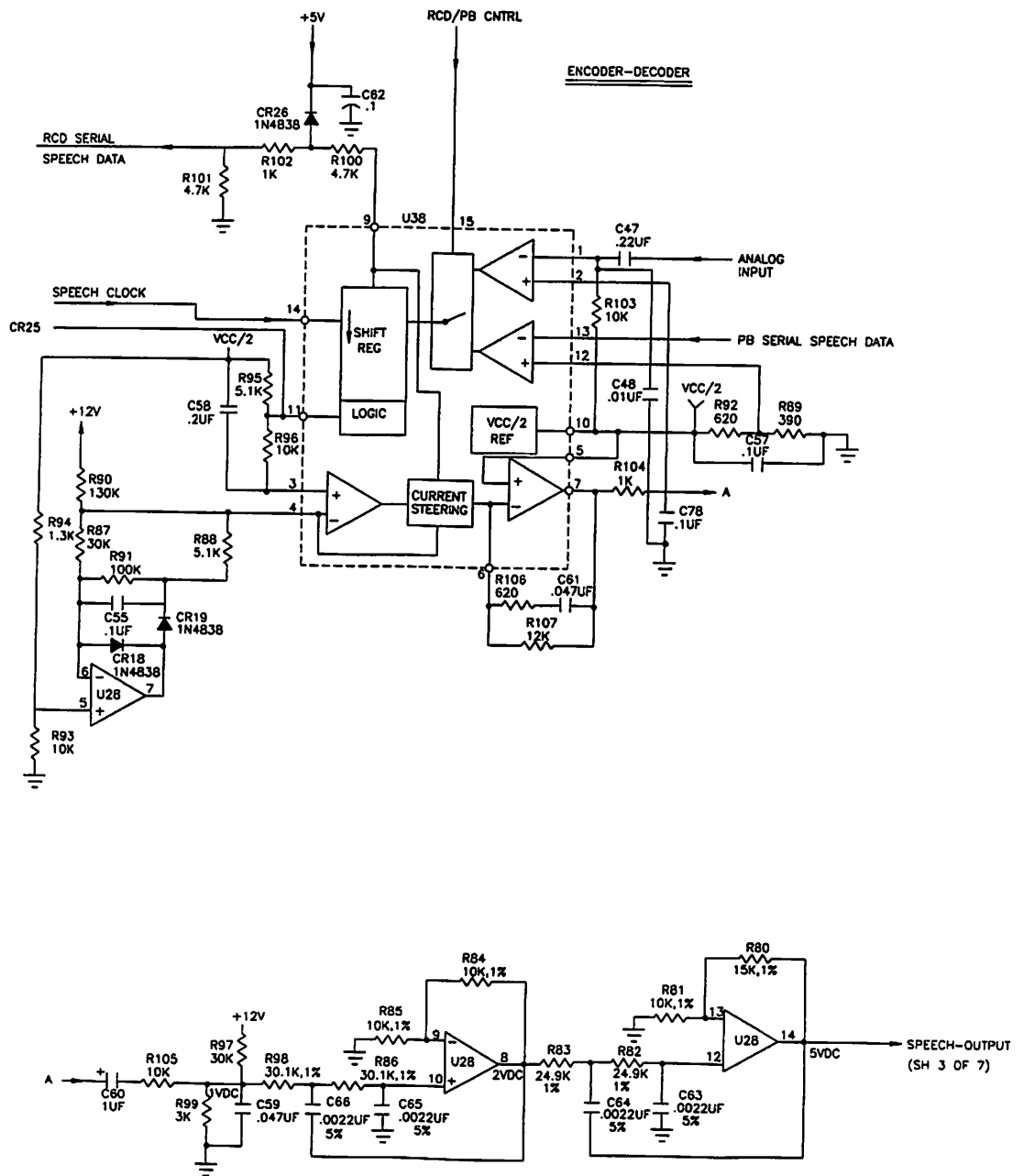
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U2	-	-	-	-
U3	-	-	-	-
U4	-	-	-	-
U5	LM239J	12	3	-
U6	LM239J	12	3	-
U7	MM54C373J	10	20	-
U8	MM54C244J	10	20	-
U9	-	-	-	-
U10	MM54C244J	10	20	-
U11	MM54C244J	10	20	-
U12	MM54C244J	10	20	-
U13	-	-	-	-
U14	MC14094BAL	8	16	-
U15	MC14073BAL	7	14	-
U16	MM54C244J	10	20	-
U17	-	-	-	-
U18	MC14022BAL	8	16	-
U19	SN54LS138J	8	16	-
U20	SN54LS244J	10	20	-
U21	MC14013BAL	7	14	-
U22	SN54LS138J	8	16	-
U23	SN54LS138J	8	16	-
U24	SN54LS02J	7	14	-
U25	LM239J	12	3	-
U26	LM239J	12	3	-
U27	-	-	-	-
U28	LM244J	11	14	4
U29	CD4047	7	14	-
U30	-	-	-	-
U31	MM54C373J	10	20	-
U32	MC14014BAL	8	16	-
U33	SN54LS244J	10	20	-
U34	MM54C373J	10	20	-
U35	SN54LS32J	7	14	-
U36	SN54LS38J	7	14	-
U37	LM380	7	14	14
U38	MC3517	8	16	16

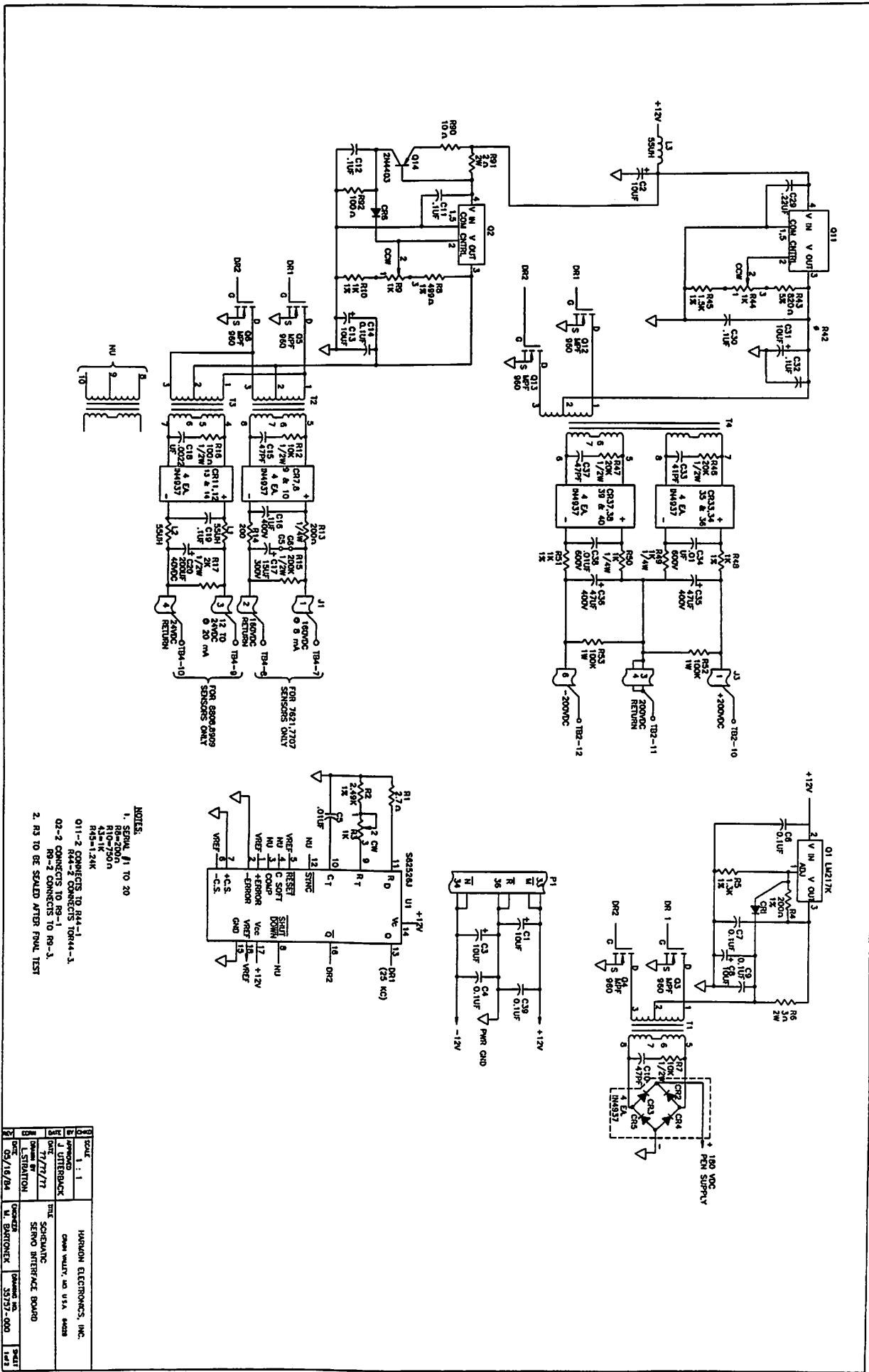
SPARE GATES

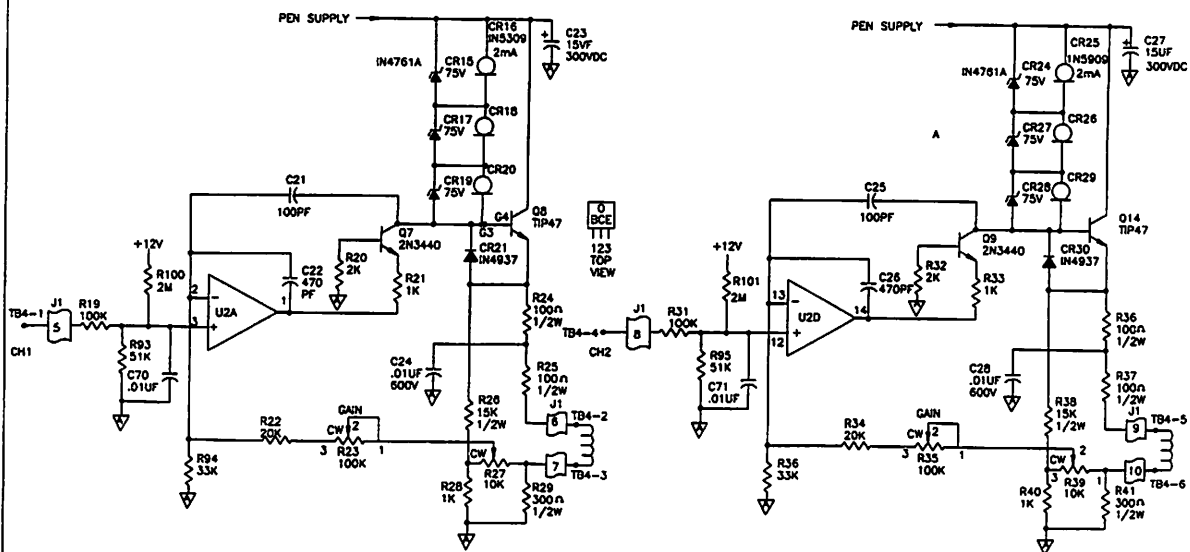
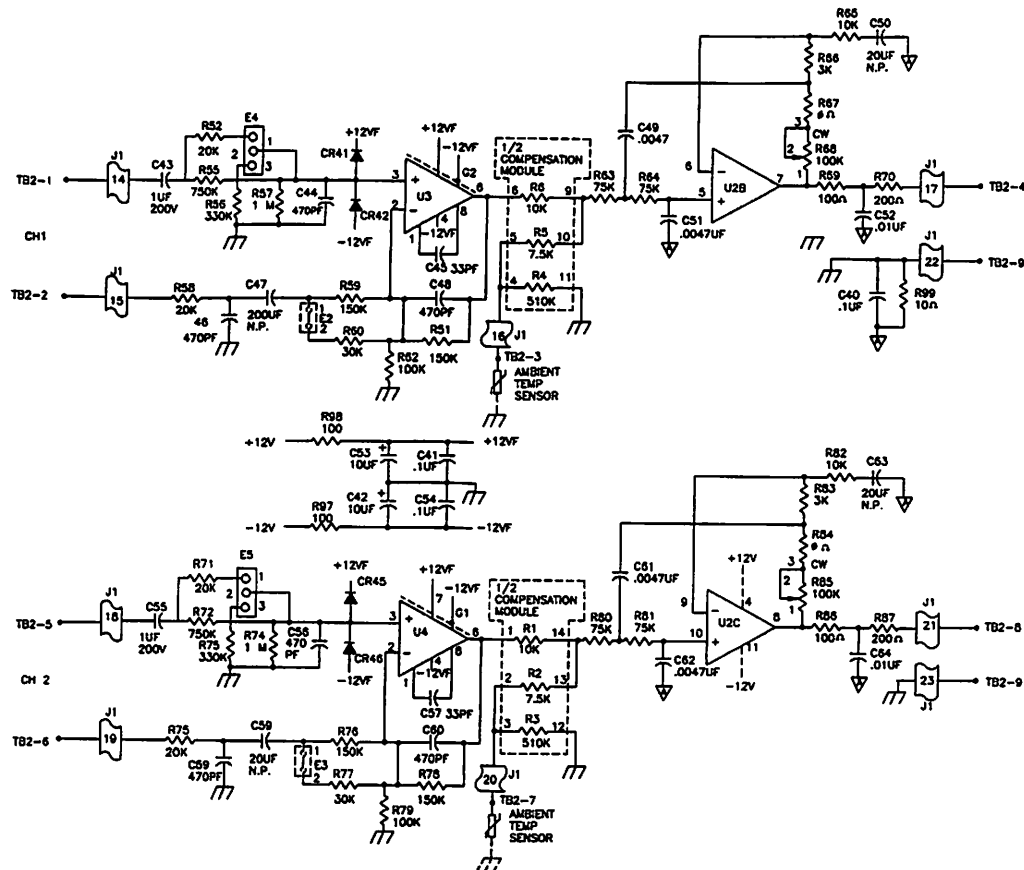


COMPONENT REF DES		
FIRST	LAST	UNUSED
C1	C78	C38-C46,C49,C52
CR1	CR28	C49,C52
R1	R126	R32,R40,R41,R61-R74, R76,R77,R78,R79
Q1	Q9	
P1	P2	
S1	S3	
J1	J2	J4
U1	U38	U2,U3,U4,U9,U13,U17,U30 U27
K1	K1	









SERVO INTERFACE BOARD

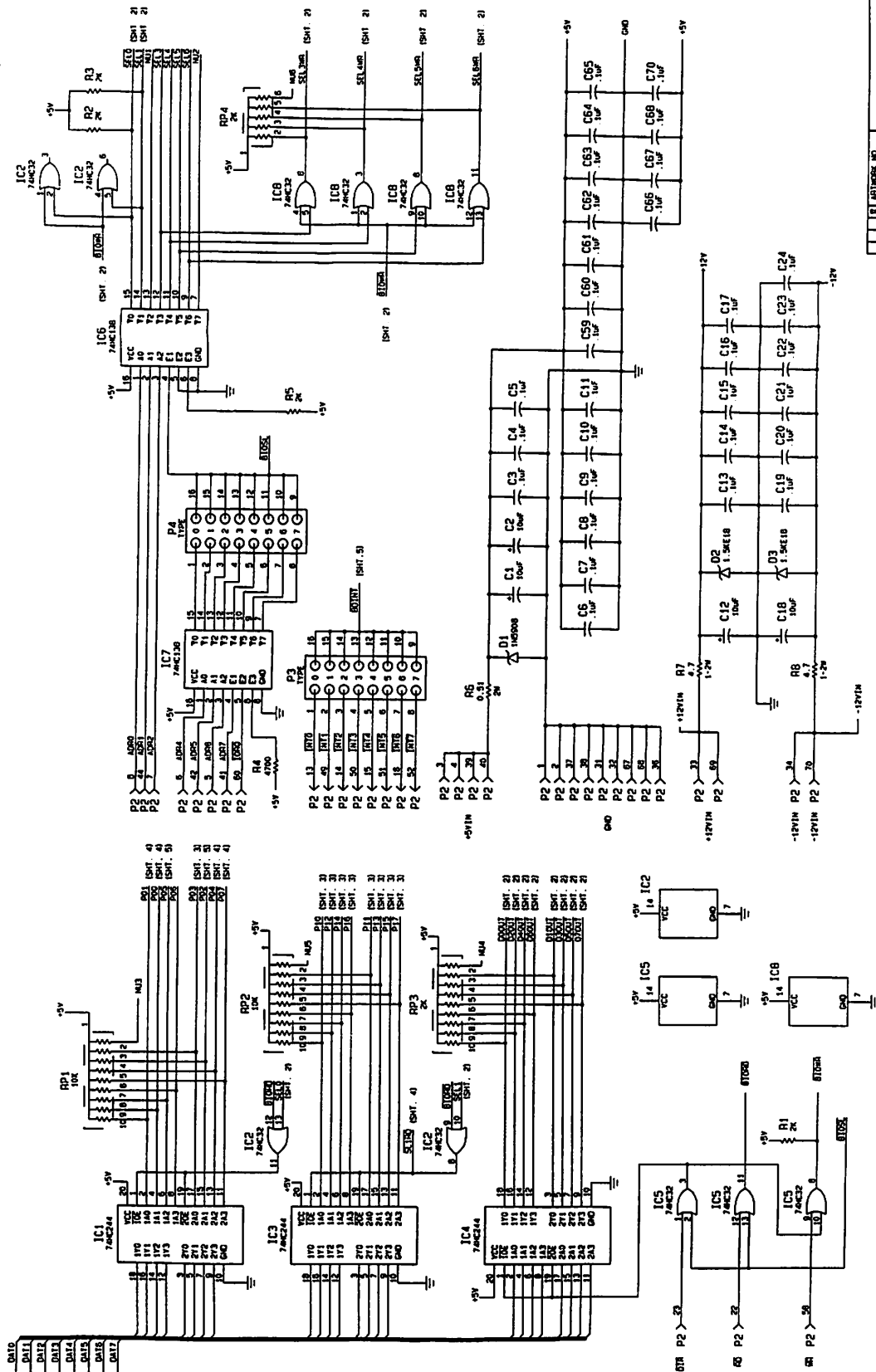
GAIN JUMPERS FOR DIFFERENT DETECTOR SYSTEMS

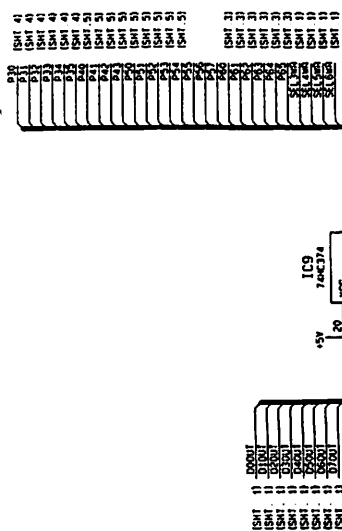
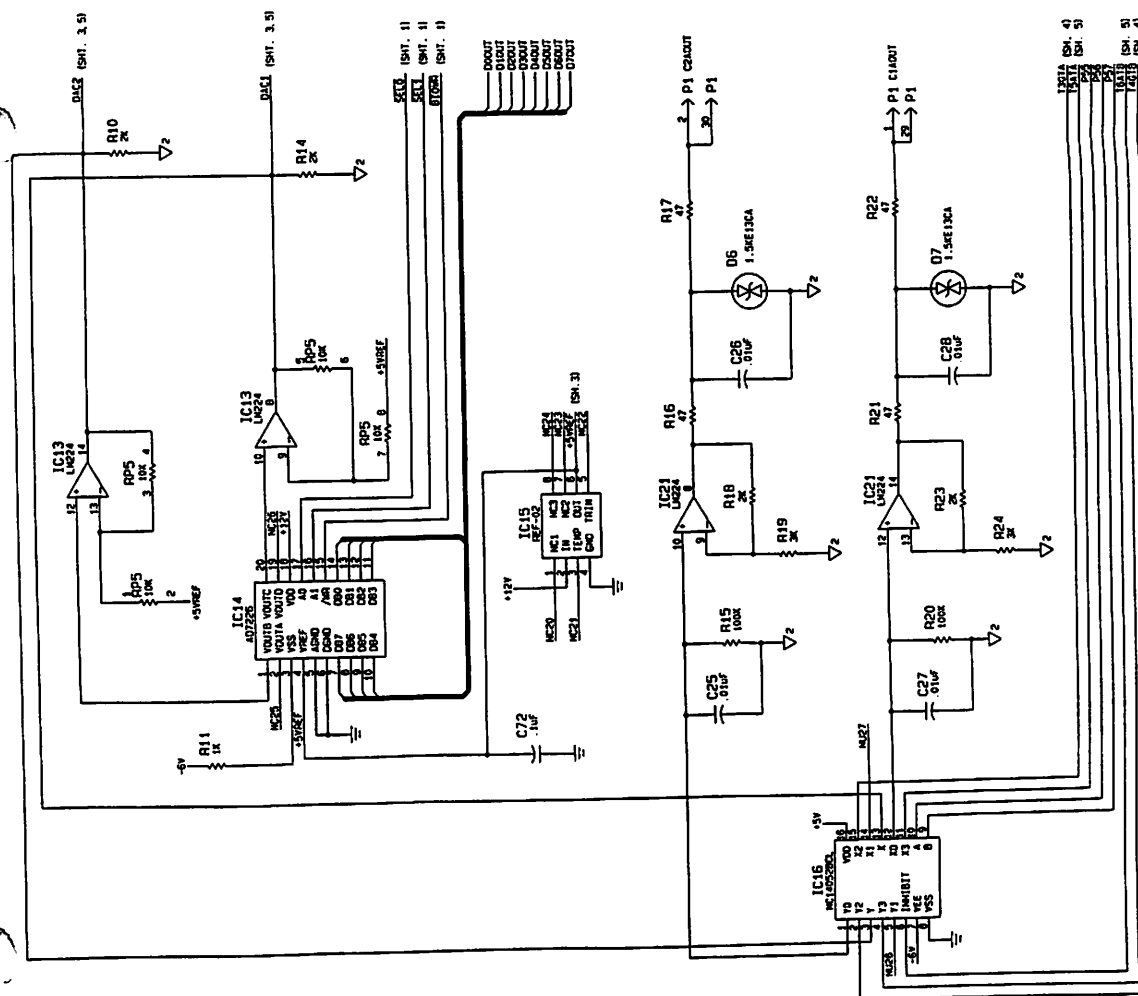
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SERVO 7621	1	2	1	2	3
SERVO 7707	1	2	1	2	3
SERVO 8808	1	2	1	2	3
SERVO 8809	1	2	1	2	3
SERVO 8809G	1	2	1	2	3

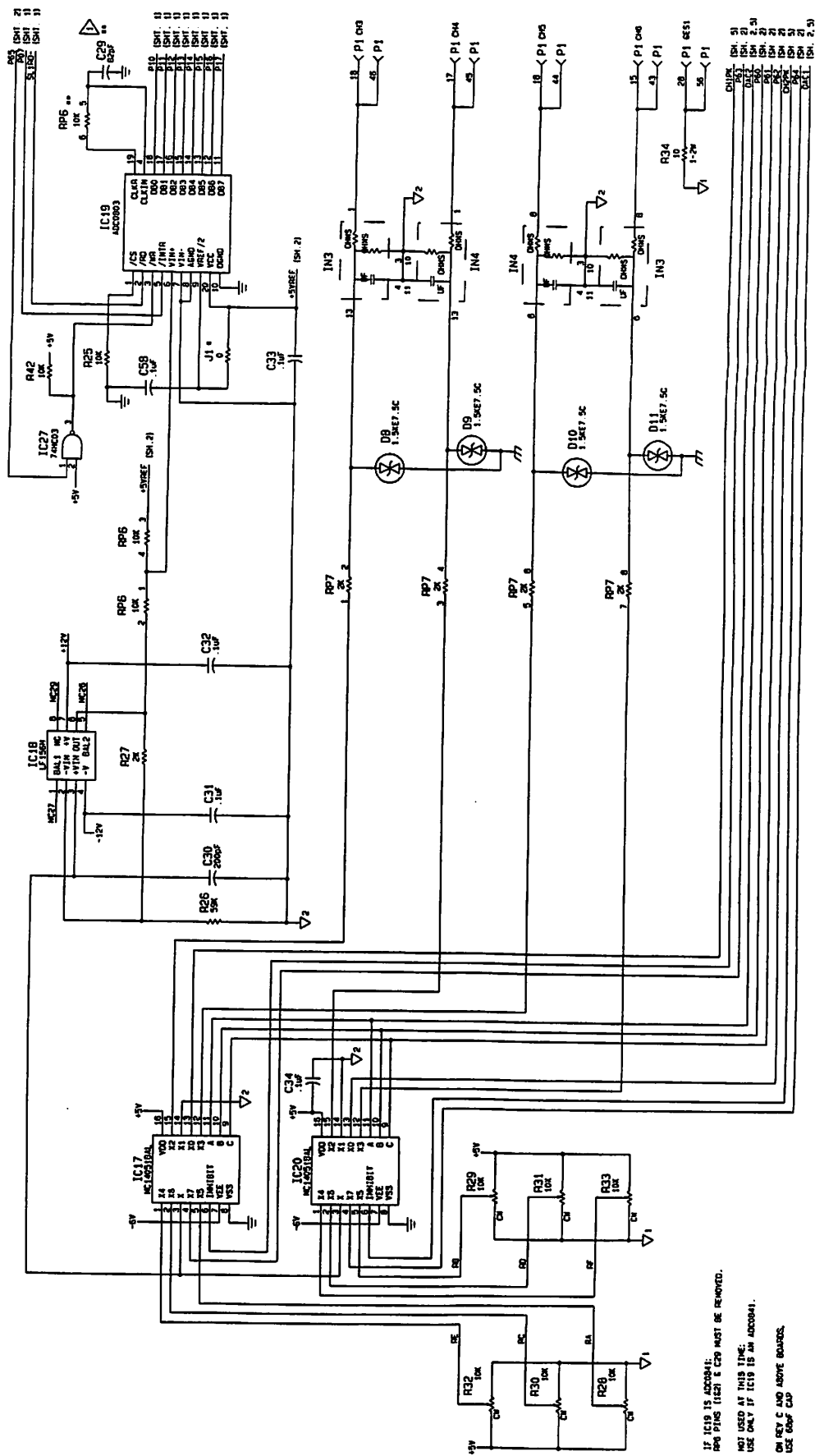
WIRE #	CONNECTION
1	TB2-3
2	TB2-7
3	GND

LAST USED	NOT USED
C71	C65-C69
R101	R88, R89, R11, R18, R30
CR46	CR22, CR23
U4	CR31, CR32
TS	CR43, CR44
O14	
L3	
E5	

SCALE 1 : 1	HARMON ELECTRONICS, INC.
APPROVED M. BARTONEK	ORAN VALLEY, MO. U.S.A. 64229
DATE 10/10/92	TITLE SERVO INTERFACE BOARD
DRAWN BY CALAY/DRAFT	DESIGNED BY M. BARTONEK
DATE 10/10/92	DRAWING NO. 35757-000
	SHEET 2 of 2

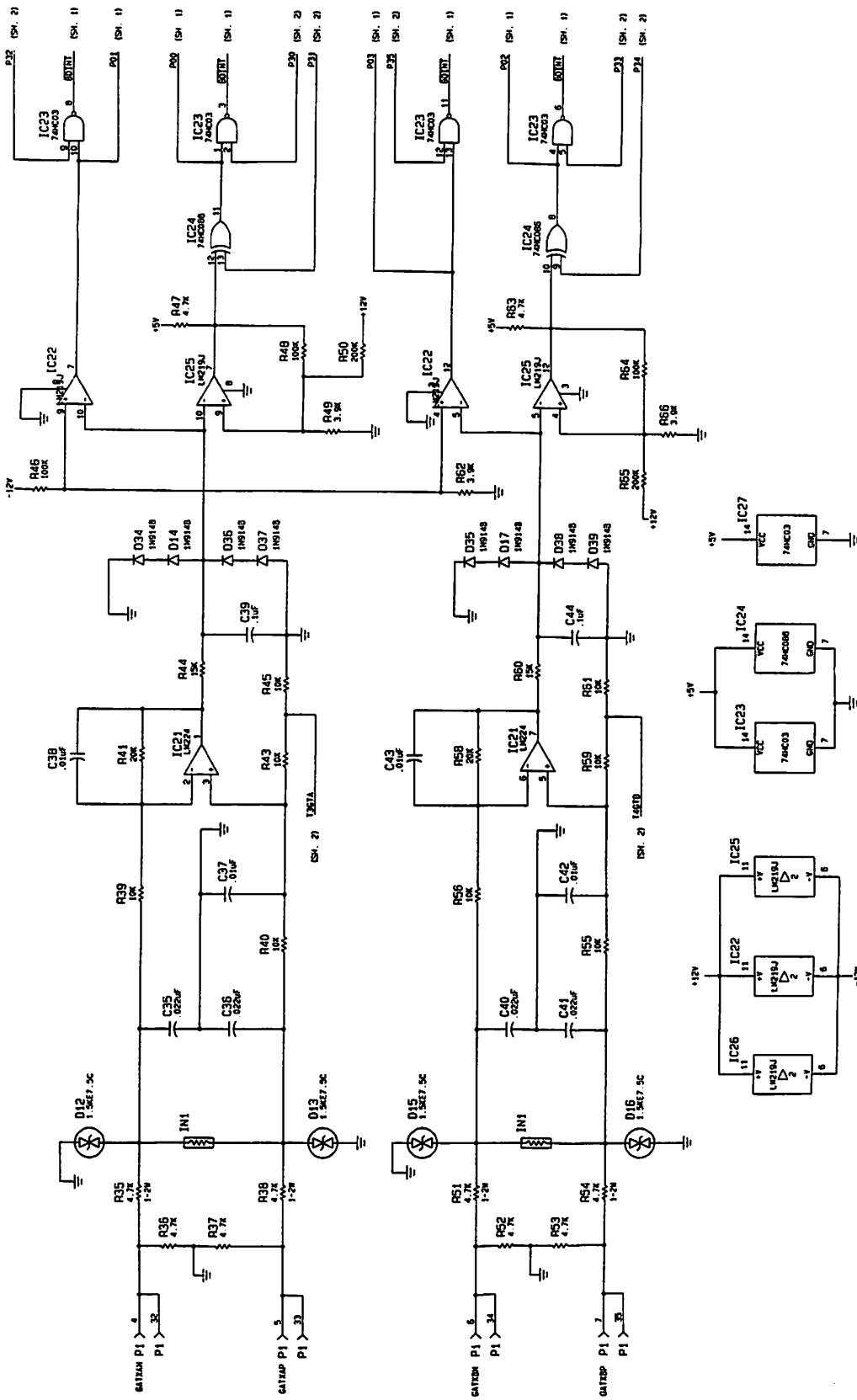
[illegible]

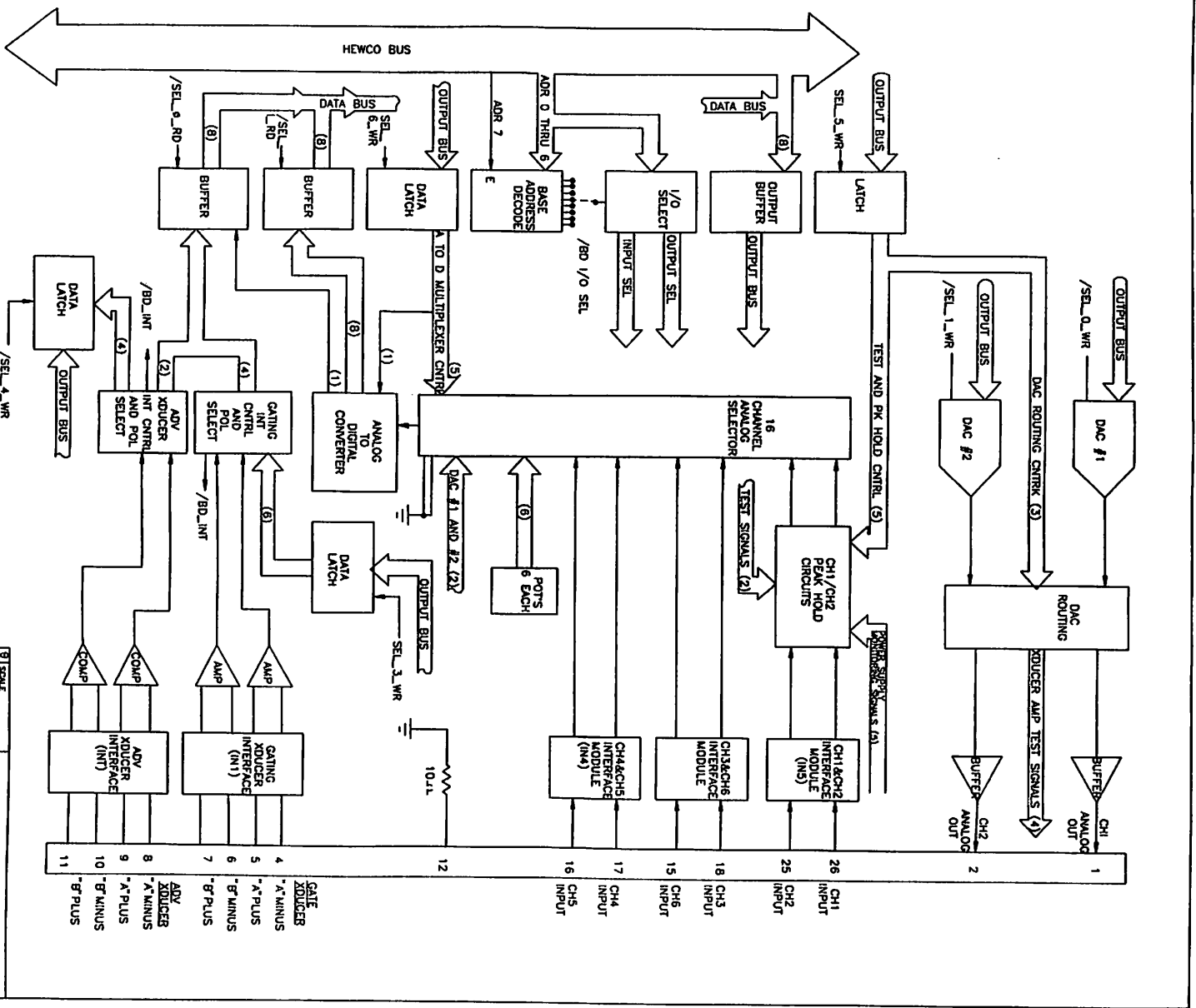




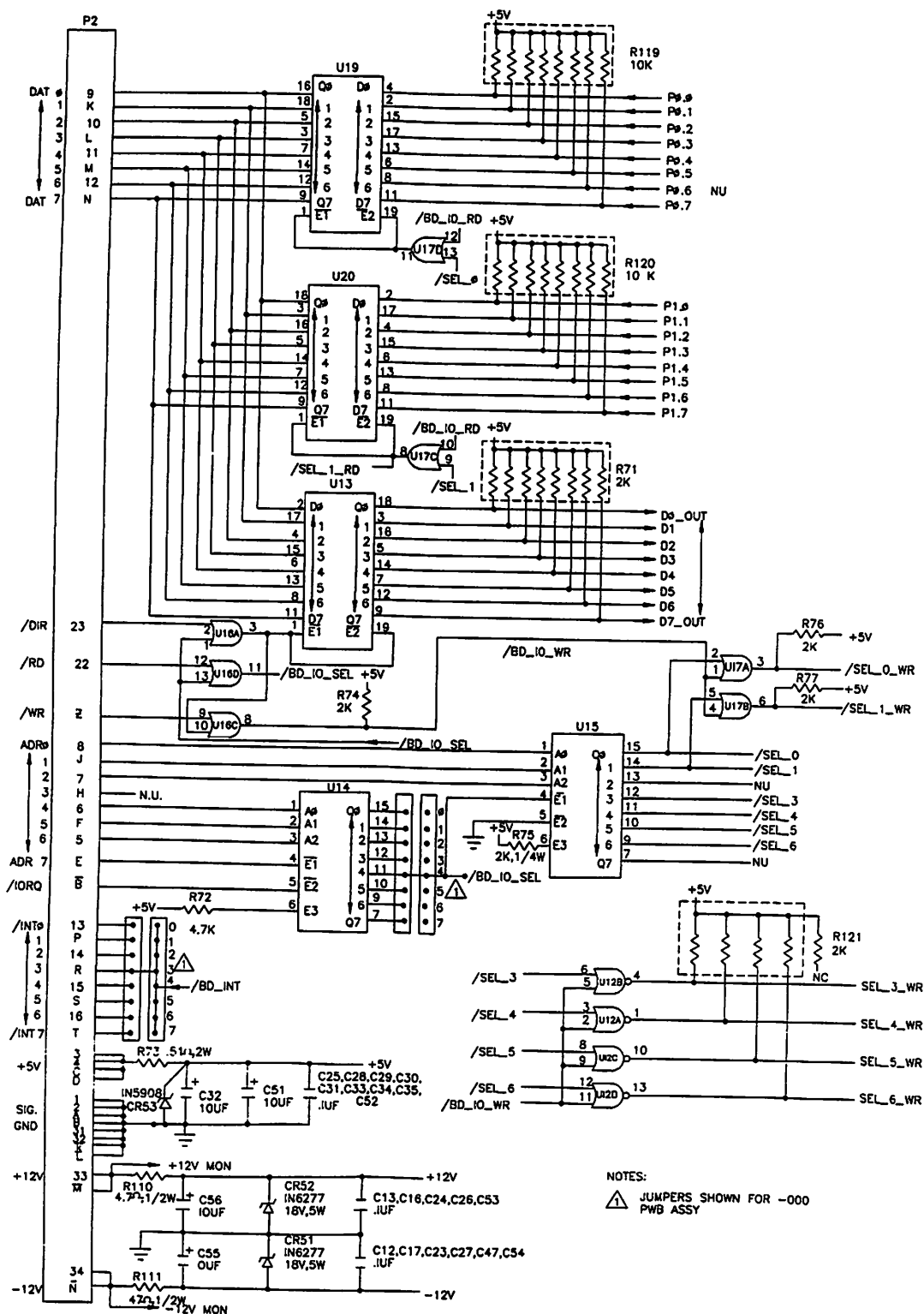
** IF IC19 IS ADDRESS:
PINS PINS (128) & C29 MUST BE REMOVED.
P NOT USED AT THIS TIME.
USE ONLY IF IC19 IS AN ADDRESS.
ON KEY C AND ABOVE BOARD.
USE 0.01" CAP

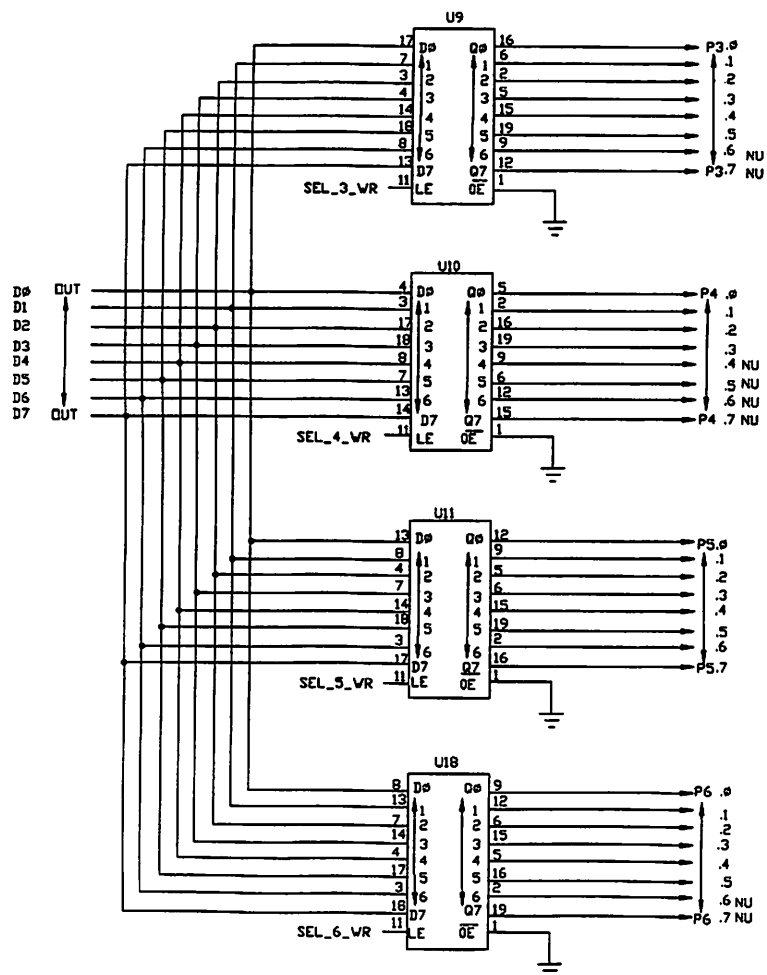
ASSY WCO-2 ANALOG BOARD
HARMON ELECTRONICS, INC.
GAIN VALLEY, MO. U.S.A. 64039
TITLE: ANALOG_11
BOARD: 3444411C
DRAWING NO: 75955-000
3 OF 5

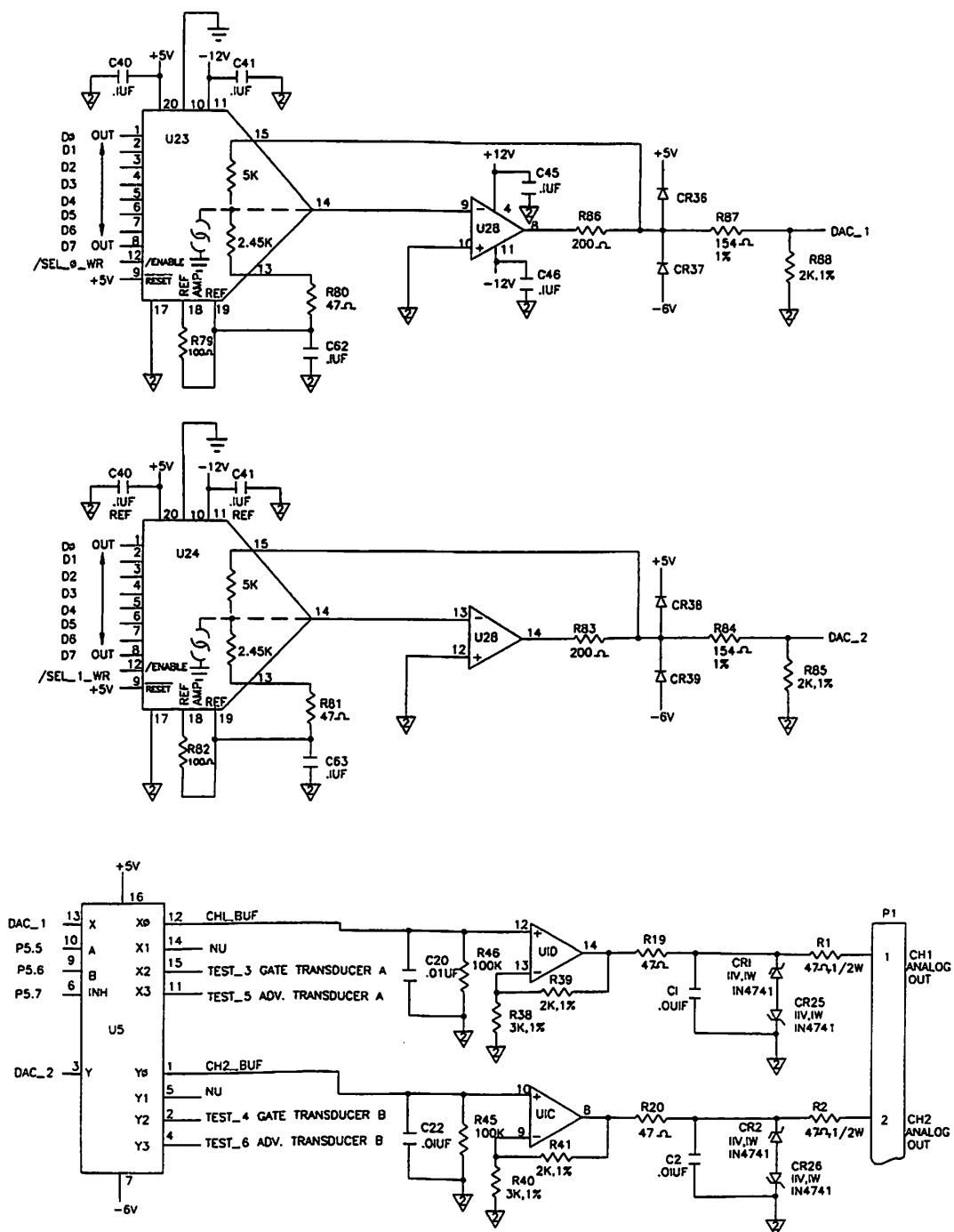


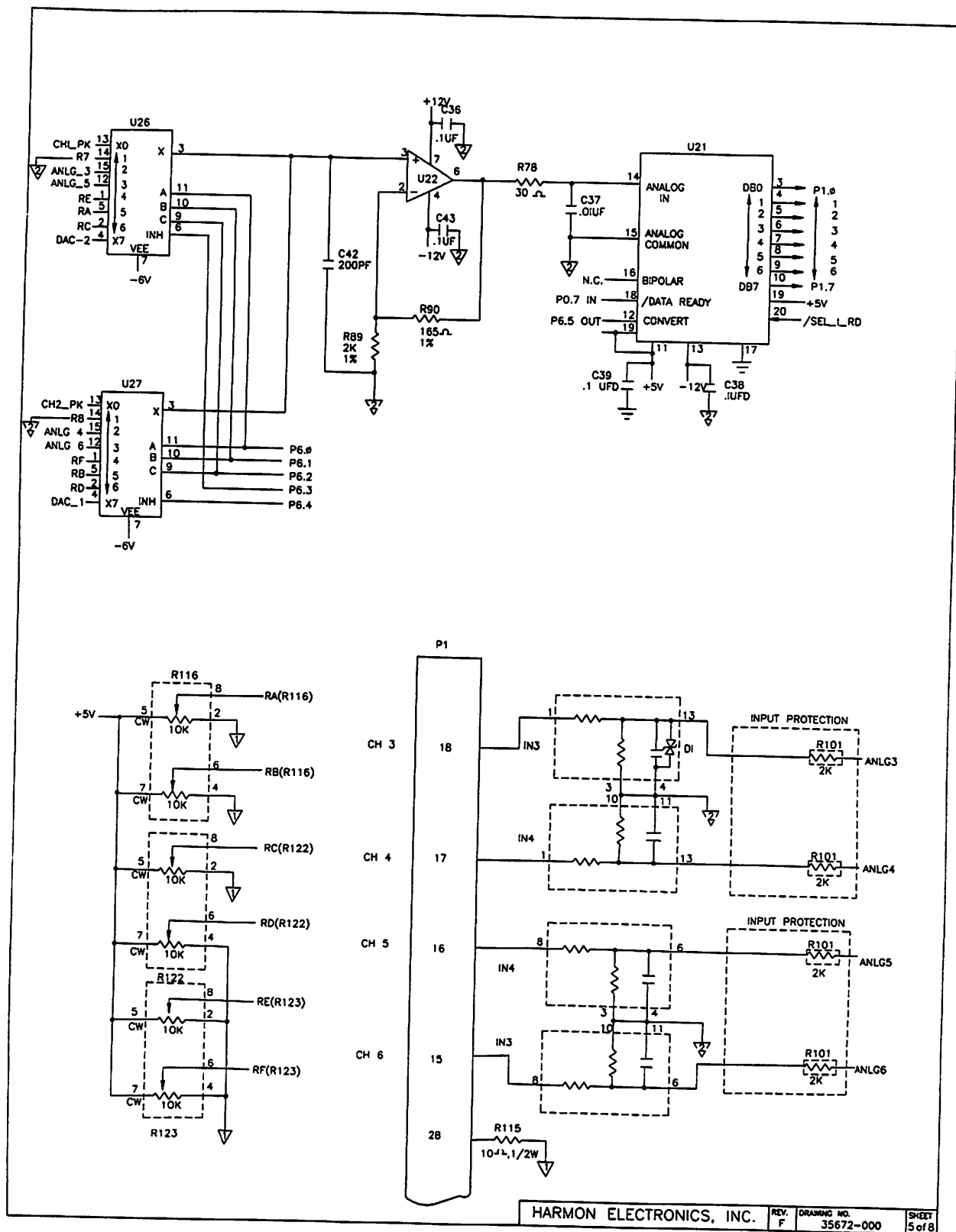


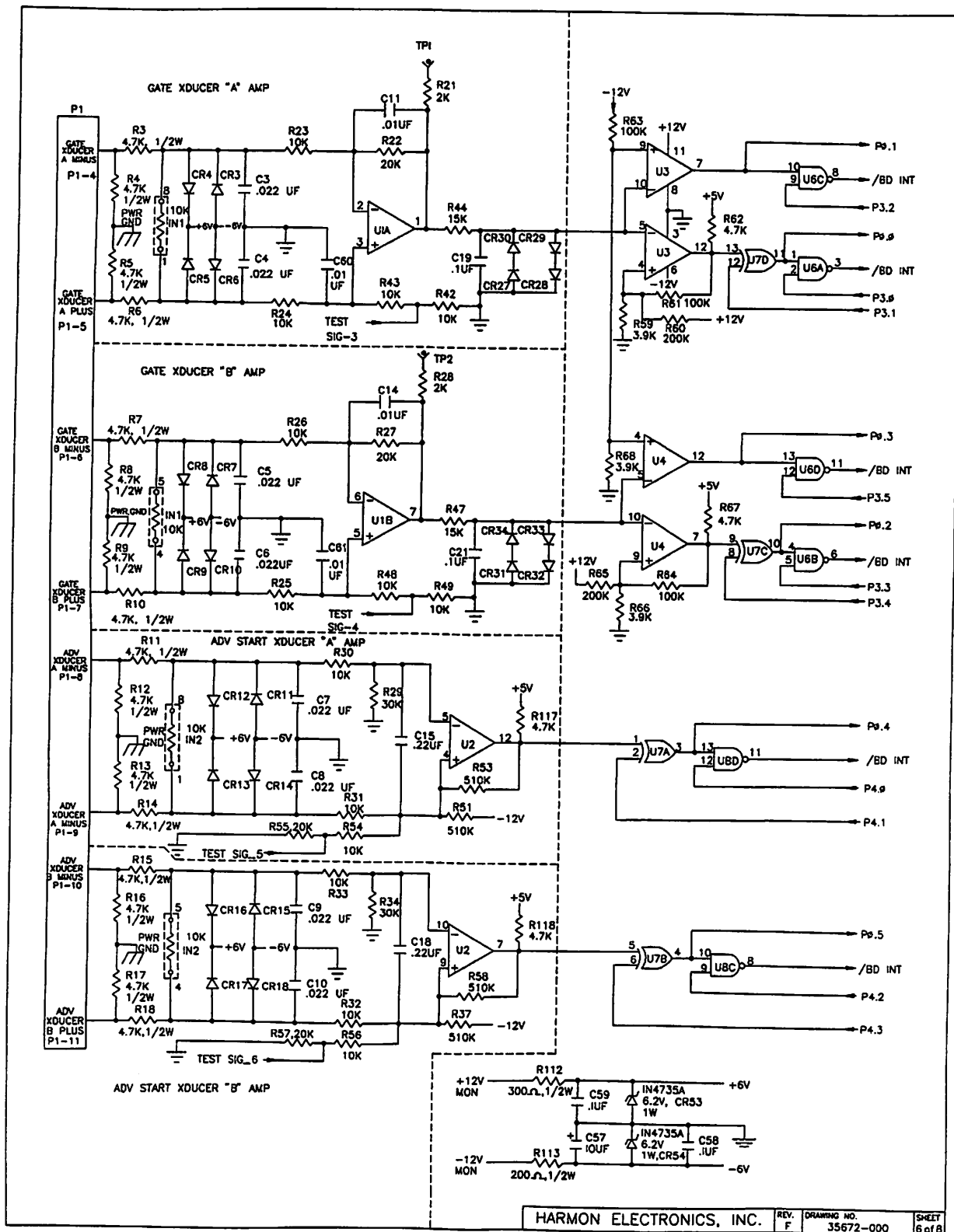
SCALE	1 : 1	HARMON ELECTRONICS, INC. CORN VALLEY, MD. U.S.A. 64029
APPROVED	DATE	
DATE	DATE	
TITLE	SCHEMATIC ANALOG BOARD	
DESIGNED BY	M. BARTONEK	
DATE	DESIGN NO.	35672-000
	SHEET	148

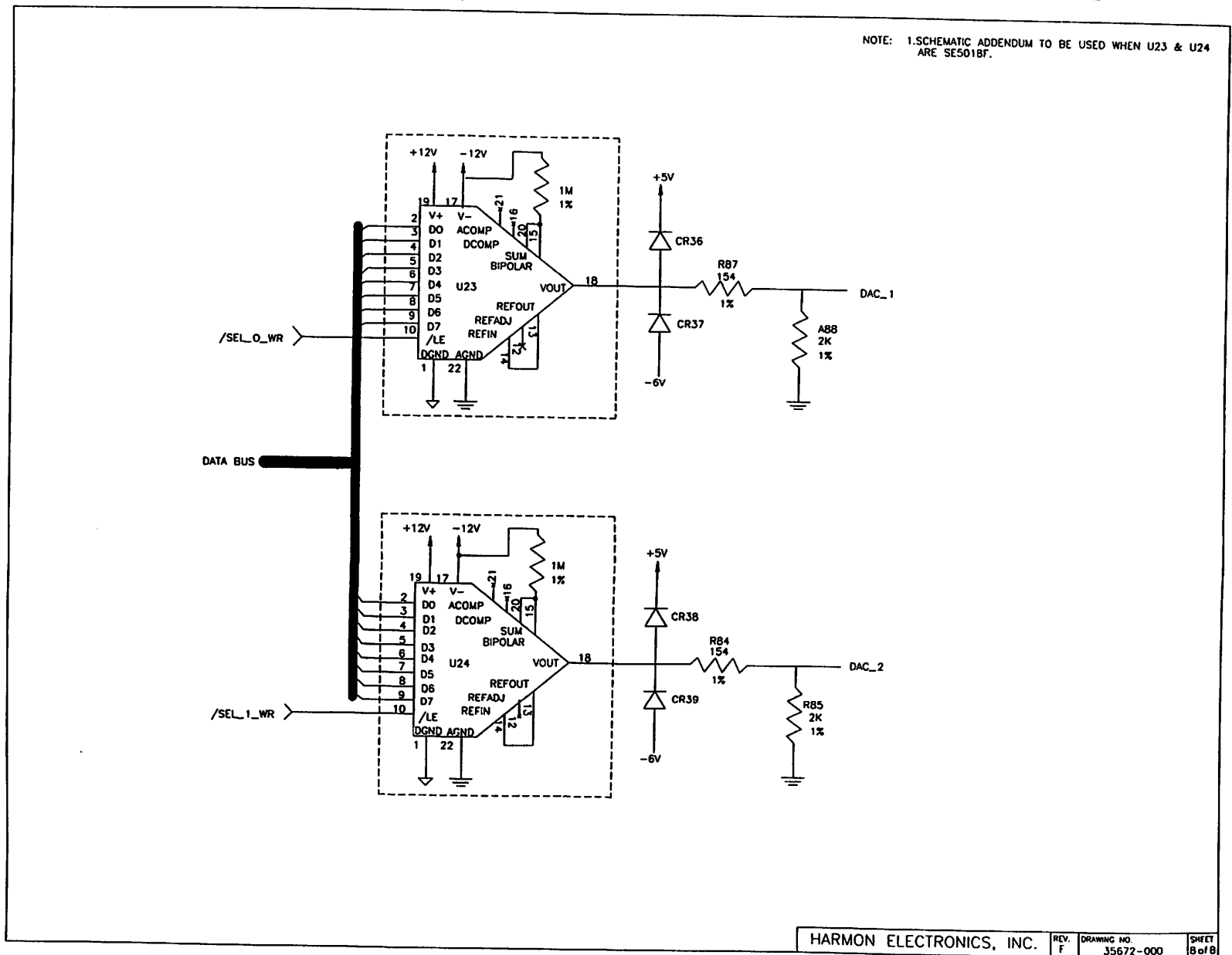


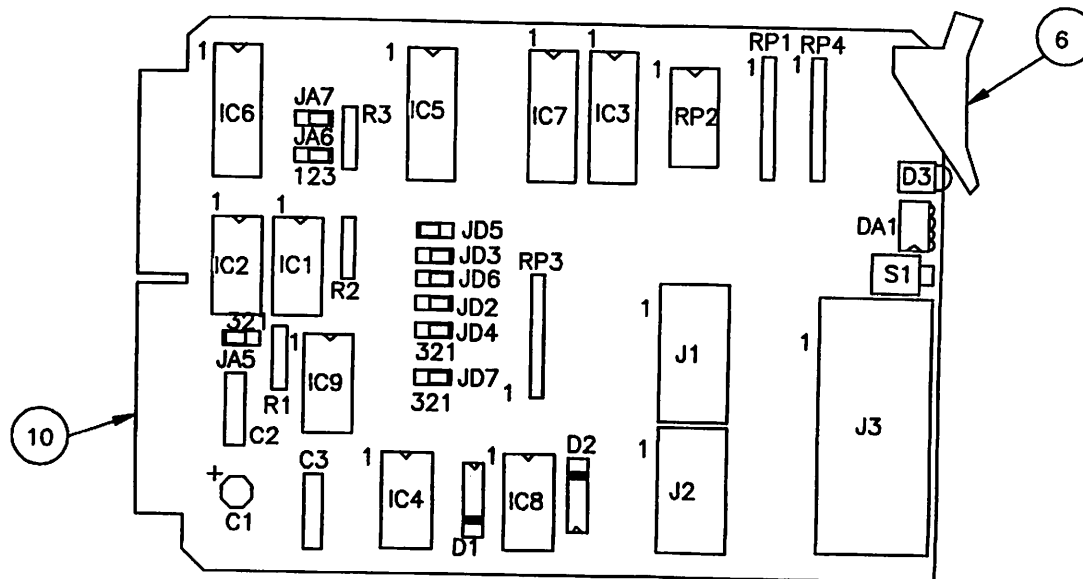






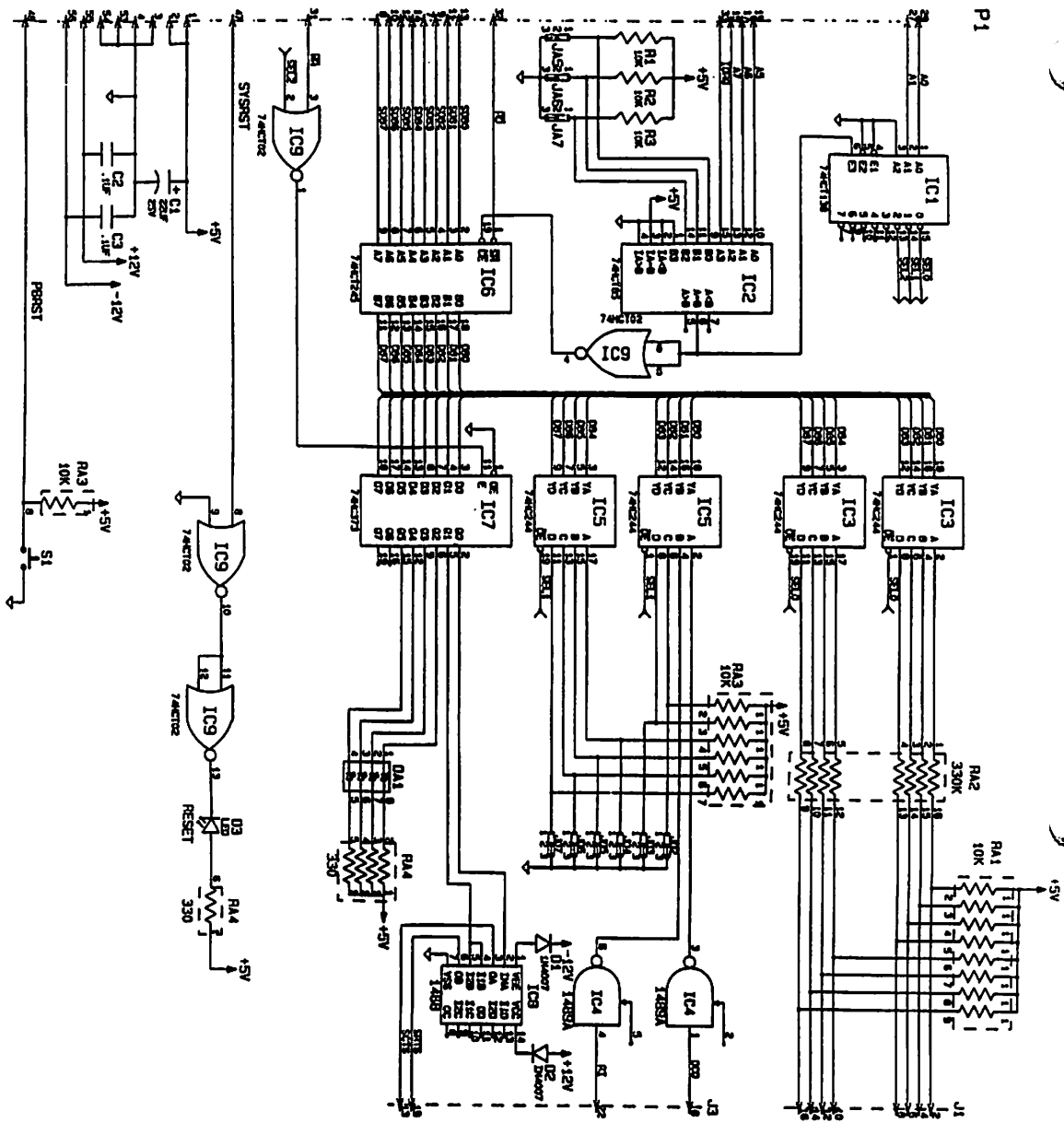




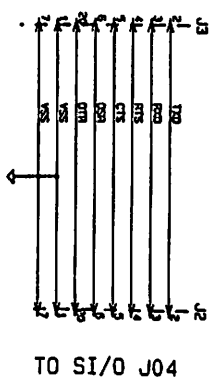


SCALE	HARMON ELECTRONICS, INC.		
	GRAIN VALLEY, MO. U.S.A. 64029		
DATE	TITLE		
1/21/87			
DRAWN BY	DCP-2		
D.LANNING			
DATE	ACCESSORY BOARD		
8/27/86			
ENGINEER	DRAWING NO.		
JOHN McNEIL			
	SHEET		
	1 of 1		

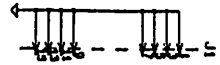
STD BUS INTERFACE



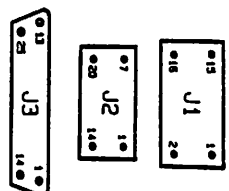
RS232 INTERFACE



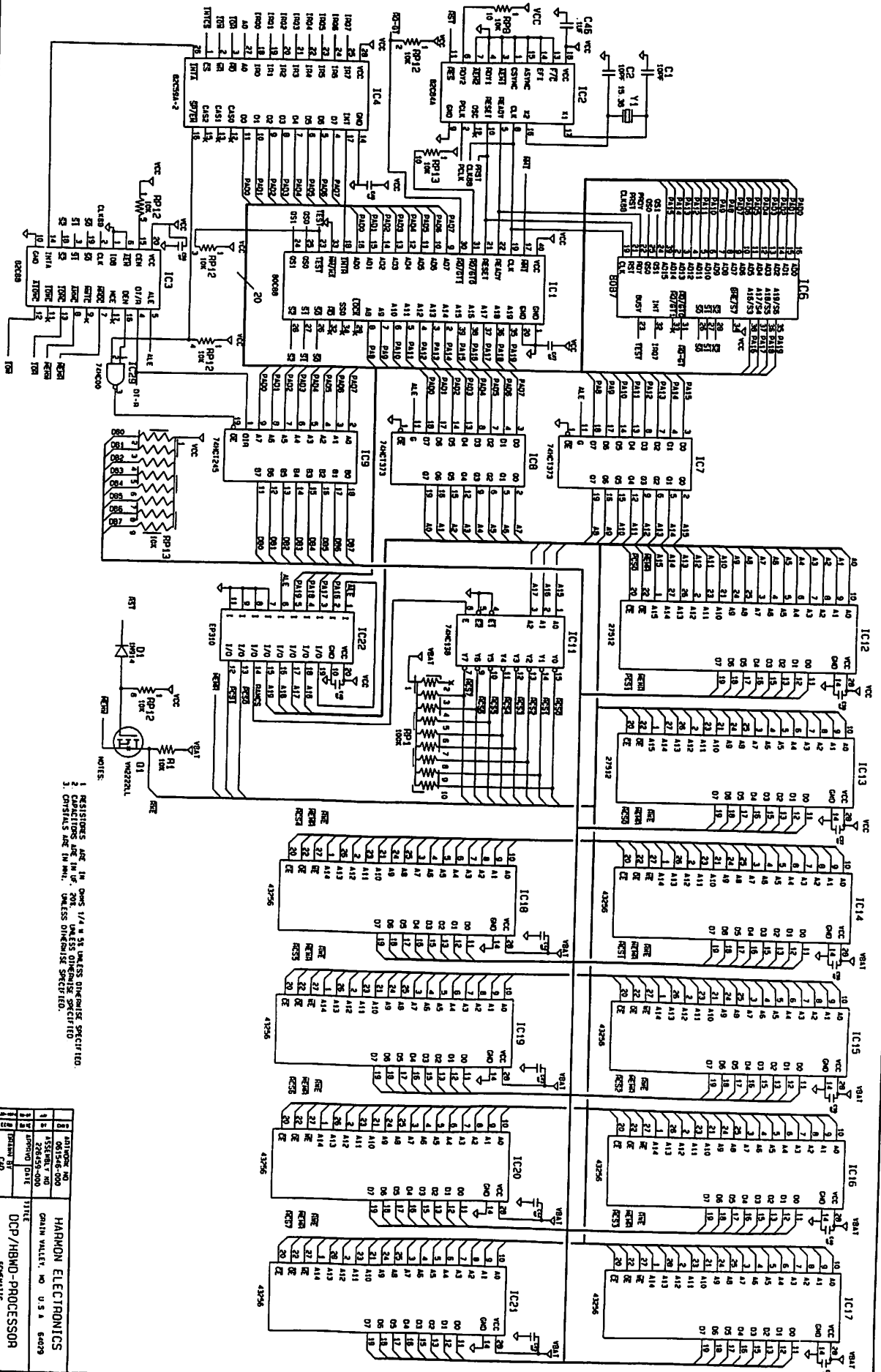
SITE STATUS



FRONT VIEW

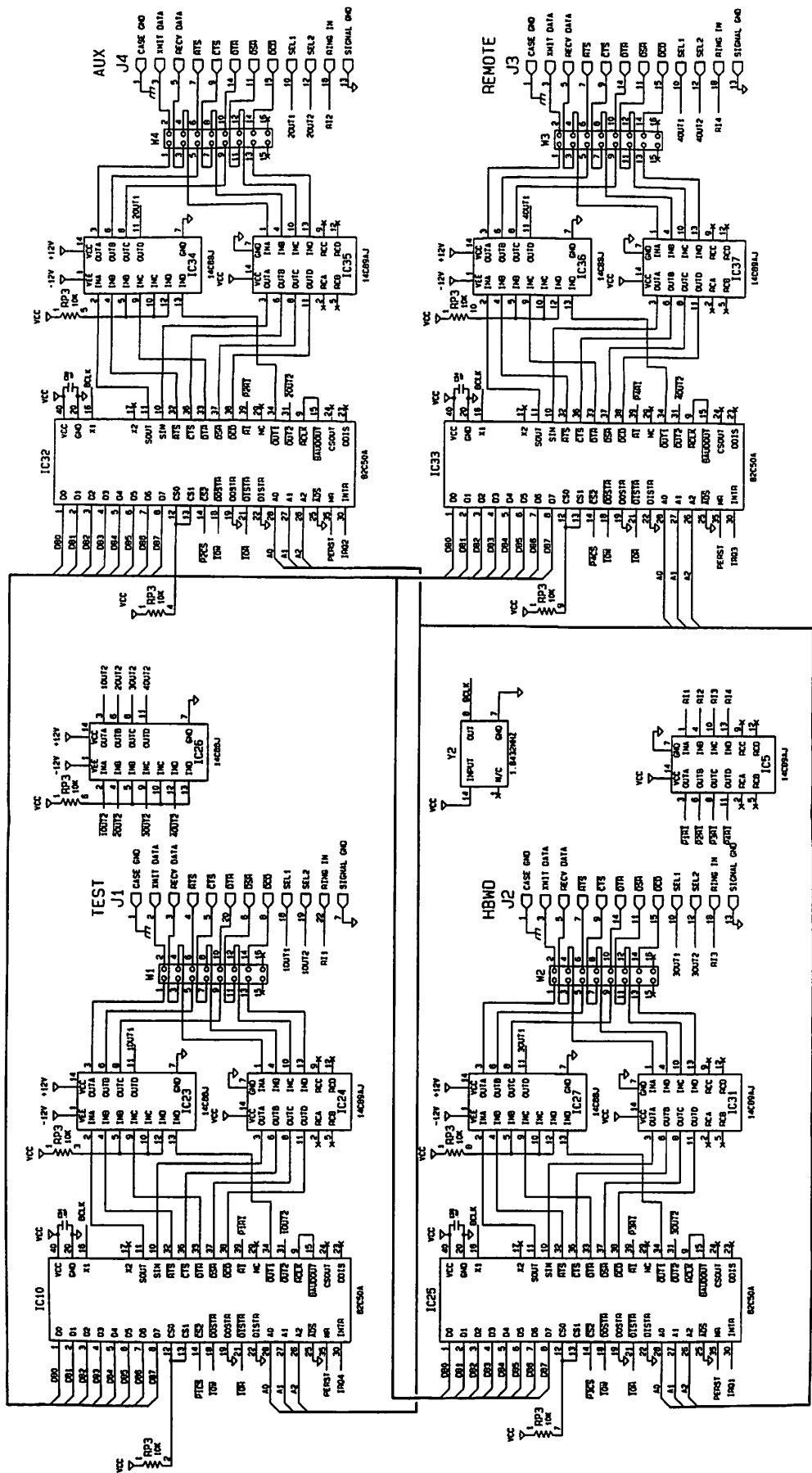


8	ARTWORK NO.	HARRON INDUSTRIES, INC.
9	ASSY NO.	6122-000
10	DATE	07/23/06
11	DESIGNED BY	DAVID J. HARRON
12	DATE	07/23/06
13	DRIVEN	DAVID J. HARRON
14	DATE	07/23/06
15	DRIVEN	DAVID J. HARRON
16	DATE	07/23/06
17	DRIVEN	DAVID J. HARRON
18	DATE	07/23/06
19	DRIVEN	DAVID J. HARRON
20	DATE	07/23/06
21	DRIVEN	DAVID J. HARRON
22	DATE	07/23/06
23	DRIVEN	DAVID J. HARRON
24	DATE	07/23/06
25	DRIVEN	DAVID J. HARRON
26	DATE	07/23/06
27	DRIVEN	DAVID J. HARRON
28	DATE	07/23/06
29	DRIVEN	DAVID J. HARRON
30	DATE	07/23/06
31	DRIVEN	DAVID J. HARRON
32	DATE	07/23/06
33	DRIVEN	DAVID J. HARRON
34	DATE	07/23/06
35	DRIVEN	DAVID J. HARRON
36	DATE	07/23/06
37	DRIVEN	DAVID J. HARRON
38	DATE	07/23/06
39	DRIVEN	DAVID J. HARRON
40	DATE	07/23/06
41	DRIVEN	DAVID J. HARRON
42	DATE	07/23/06
43	DRIVEN	DAVID J. HARRON
44	DATE	07/23/06
45	DRIVEN	DAVID J. HARRON
46	DATE	07/23/06
47	DRIVEN	DAVID J. HARRON
48	DATE	07/23/06
49	DRIVEN	DAVID J. HARRON
50	DATE	07/23/06
51	DRIVEN	DAVID J. HARRON
52	DATE	07/23/06
53	DRIVEN	DAVID J. HARRON
54	DATE	07/23/06
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56	DATE	07/23/06
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58	DATE	07/23/06
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60	DATE	07/23/06
61	DRIVEN	DAVID J. HARRON
62	DATE	07/23/06
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64	DATE	07/23/06
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78	DATE	07/23/06
79	DRIVEN	DAVID J. HARRON
80	DATE	07/23/06
81	DRIVEN	DAVID J. HARRON
82	DATE	07/23/06
83	DRIVEN	DAVID J. HARRON
84	DATE	07/23/06
85	DRIVEN	DAVID J. HARRON
86	DATE	07/23/06
87	DRIVEN	DAVID J. HARRON
88	DATE	07/23/06
89	DRIVEN	DAVID J. HARRON
90	DATE	07/23/06
91	DRIVEN	DAVID J. HARRON
92	DATE	07/23/06
93	DRIVEN	DAVID J. HARRON
94	DATE	07/23/06
95	DRIVEN	DAVID J. HARRON
96	DATE	07/23/06
97	DRIVEN	DAVID J. HARRON
98	DATE	07/23/06
99	DRIVEN	DAVID J. HARRON
100	DATE	07/23/06



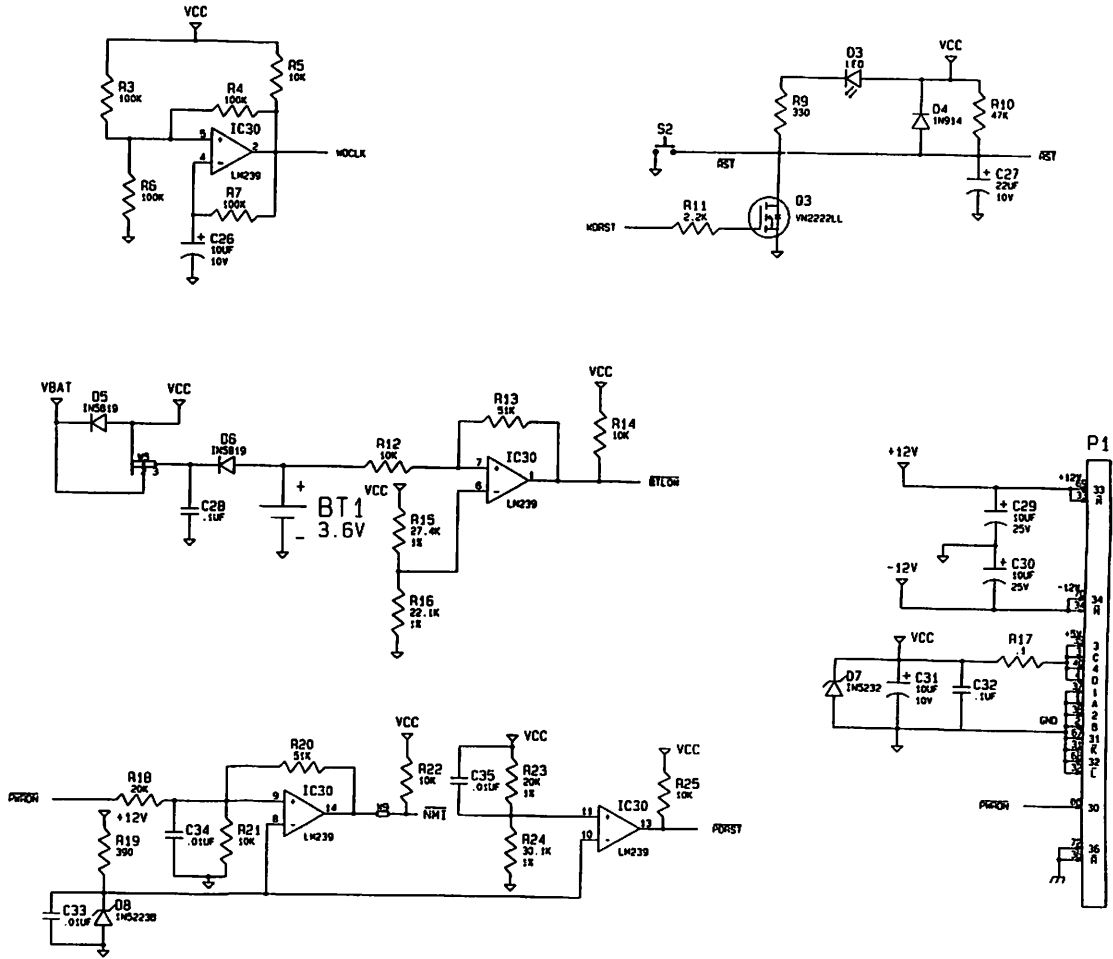
1	74180	Hex Inverter	1
2	74180	Hex Inverter	1
3	74180	Hex Inverter	1
4	74180	Hex Inverter	1
5	74180	Hex Inverter	1
6	74180	Hex Inverter	1
7	74180	Hex Inverter	1
8	74180	Hex Inverter	1
9	74180	Hex Inverter	1
10	74180	Hex Inverter	1
11	74180	Hex Inverter	1
12	74180	Hex Inverter	1
13	74180	Hex Inverter	1
14	74180	Hex Inverter	1
15	74180	Hex Inverter	1
16	74180	Hex Inverter	1
17	74180	Hex Inverter	1
18	74180	Hex Inverter	1
19	74180	Hex Inverter	1
20	74180	Hex Inverter	1
21	74180	Hex Inverter	1

HARRISON ELECTRONICS
 GAIN VALLEY, MO U.S.A. 64079
 DCP/HBMD-PROCESSOR
 1994-01-07
 1994-01-07



ARTWORK NO.	081548-000	HARMON ELECTRONICS GRAIN VALLEY, MO U.S.A. 64079	TITLE DCP/HBWD-PROCESSOR	ENGINEER SCHEMATIC	DATE 01-04-87	JOB NO. 10993-000	SHEET 2 of 4
ASSEMBLY NO.	081548-000						
REVISION DATE	081548-000						

REF.	DES.	DEVICE	TYPE	QDND	VBAT	VCC	+12V	-12V	BYPASS	VALUE
IC1		80C88		20		40			C47	.10UF
IC2		82C84A		18	9				C46	.10UF
IC3		82C88		10		20			C50	.10UF
IC4		82C59A-2		14		28			C48	.10UF
IC5		14C89AJ		7	14				NONE	0
IC6		8087		20		40			C59	.10UF
IC7		74HC1373		10		20			C60	.10UF
IC8		74HC1373		10		20			C61	.10UF
IC9		74HC1245		10		20			C62	.10UF
IC10		82C50		20		40			C51	.10UF
IC11		74HC138		8	16				C63	.10UF
IC12		27512		14		28			C36	.10UF
IC13		27512		14		28			C37	.10UF
IC14		43256		14	28				C38	.10UF
IC15		43256		14	28				C39	.10UF
IC16		43256		14	28				C40	.10UF
IC17		43256		14	28				C41	.10UF
IC18		43256		14	28				C42	.10UF
IC19		43256		14	28				C43	.10UF
IC20		43256		14	28				C44	.10UF
IC21		43256		14	28				C45	.10UF
IC22		EP310		10		20			C49	.10UF
IC23		14C88J				14	1		NONE	0
IC24		14C89AJ		7	14				NONE	0
IC25		82C50		20		40			C53	.10UF
IC26		14C88J				14	1		NONE	0
IC27		14C88J				14	1		NONE	0
IC28		NOT-USED							NONE	0
IC29		74HC00		7	14				C64	.10UF
IC30		LM239		12	3				C65	.10UF
IC31		14C89AJ		7	14				NONE	0
IC32		82C50		20		40			C52	.10UF
IC33		82C50		20		40			C54	.10UF
IC34		14C88J				14	1		NONE	0
IC35		14C89AJ		7	14				NONE	0
IC36		14C88J				14	1		NONE	0
IC37		14C89AJ		7	14				NONE	0
IC38		82C54		12		24			C55	.10UF
IC39		74HC32		7	14				C66	.10UF
IC40		74HC154		12		24			C77	.10UF
IC41		74HC32		7	14				C67	.10UF
IC42		74HC1374		10		20			C68	.10UF
IC43		74HC1244		10		20			C69	.10UF
IC44		MS86242		9	18				C56	.10UF
IC45		74HC1244		10		20			C70	.10UF
IC46		EP310		10		20			C57	.10UF
IC47		EP310		10		20			C58	.10UF
IC48		74HC1244		10		20			C71	.10UF
IC49		74HC1244		10		20			C72	.10UF
IC50		74HC1244		10		20			C73	.10UF
IC51		74HC1244		10		20			C74	.10UF
IC52		74LS641		10		20			C75	.10UF
IC53		74HC120		7	14				C76	.10UF



REV	DESCRIPTION	DATE	BY	CHKD
1	ARTWORK NO. 061346-000			
2	ASSEMBLY NO. 226450-000			
3	APPROVD	DATE		
4	DRAWN BY CAD			
5	DATE 07-04-87			
6	ENGINEER UTTERBACK			
7	DRAWING NO. 35943-000			
8	SHEET 4 OF 4			

HARMON ELECTRONICS	
GRAIN VALLEY, MO U S A 64029	
TITLE	
DCP/HBWD-PROCESSOR	
SCHEMATIC	